A Fractional-N Sub-Sampling PLL using Pipelined Phase-Interpolator with a FoM of -246dB

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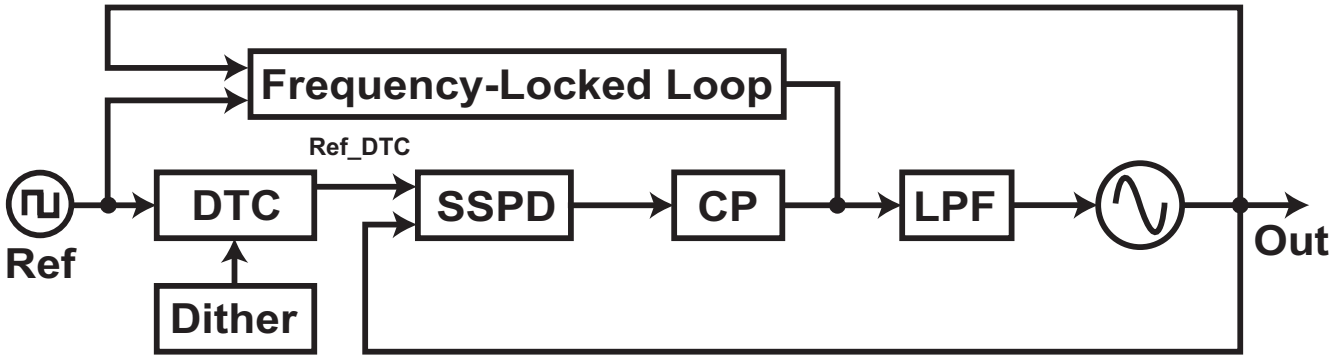
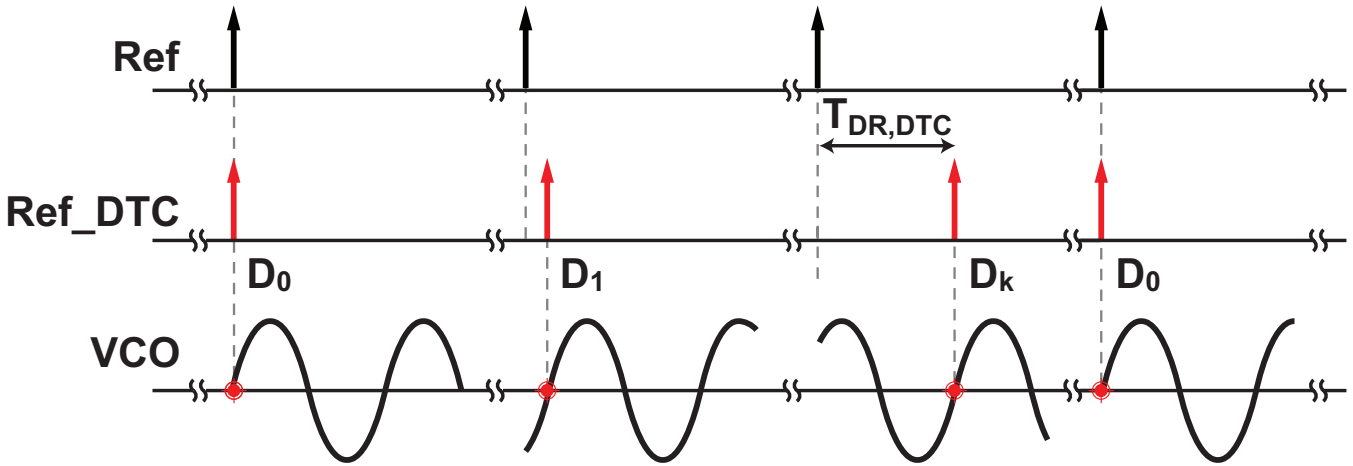
Motivation

- Wireless carrier generation requires fractional-*N* PLL.
- Fractional operation introduces additional noise.
- Conventional synthesizer architectures:
  - CP Based: Poor close-in phase noise.
  - TDC Based: Power-jitter trade-off.
  - Injection Locking: Large spurious.
  - Sub-sampling: Power-jitter tradeoff.

Aim: Low-power high-purity fractional-*N* SS-PLL

Fractional-*N* SS-PLL: Prior Art



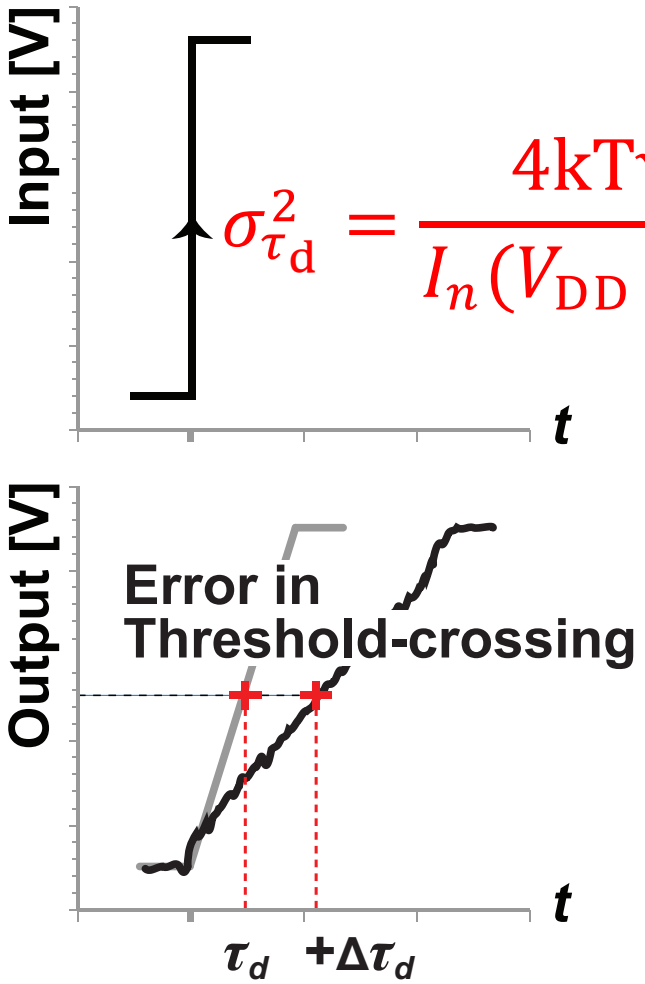


f_{out} = (N+n)×f_{ref}; N- Integer part; n- fractional part

DTC facilitates fractional-*N* operation

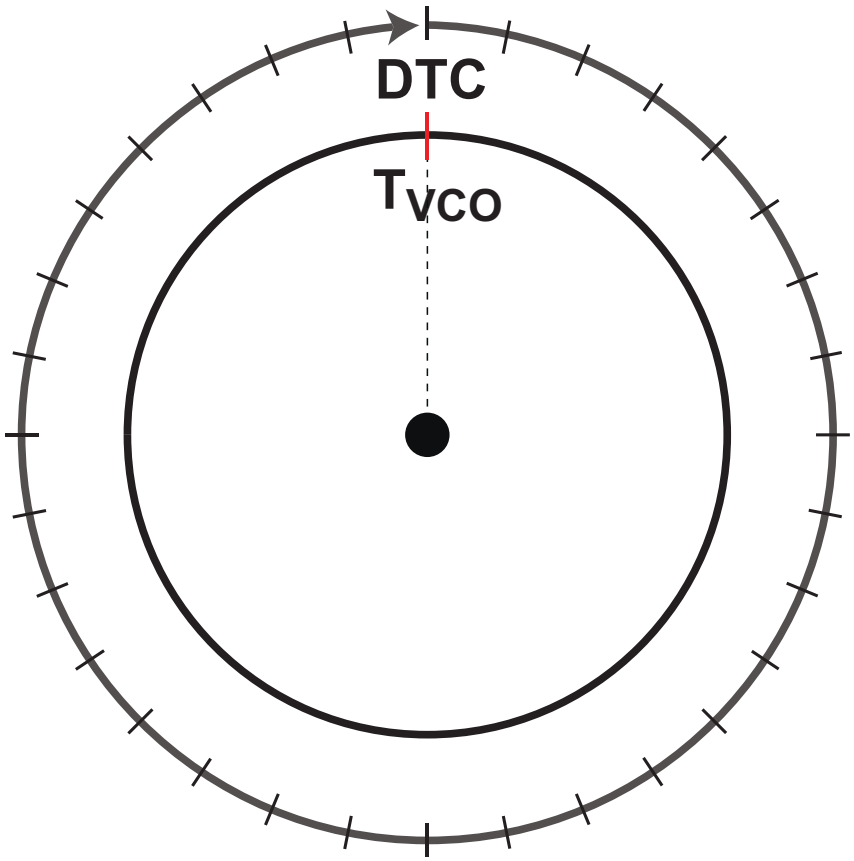
[1] G. Marucci, ISSCC 2014, [2] Po-Chun Huang, ISSCC 2014, [3] K. Raczkowski, RFIC 2014]

Conventional Frac.-*N* SSPLL: Challenges



$$\sigma_{\tau_d}^2 = \frac{4kT\gamma\,\tau_d}{I_n(V_{DD} - V_{th})}$$

[4] A. Abidi, JSSC 2006



DTC Only

$$\tau_{DR,DTC} \geq \tau_{VCO}$$

DTC only architecture requires large dynamic range

Proposed Technique

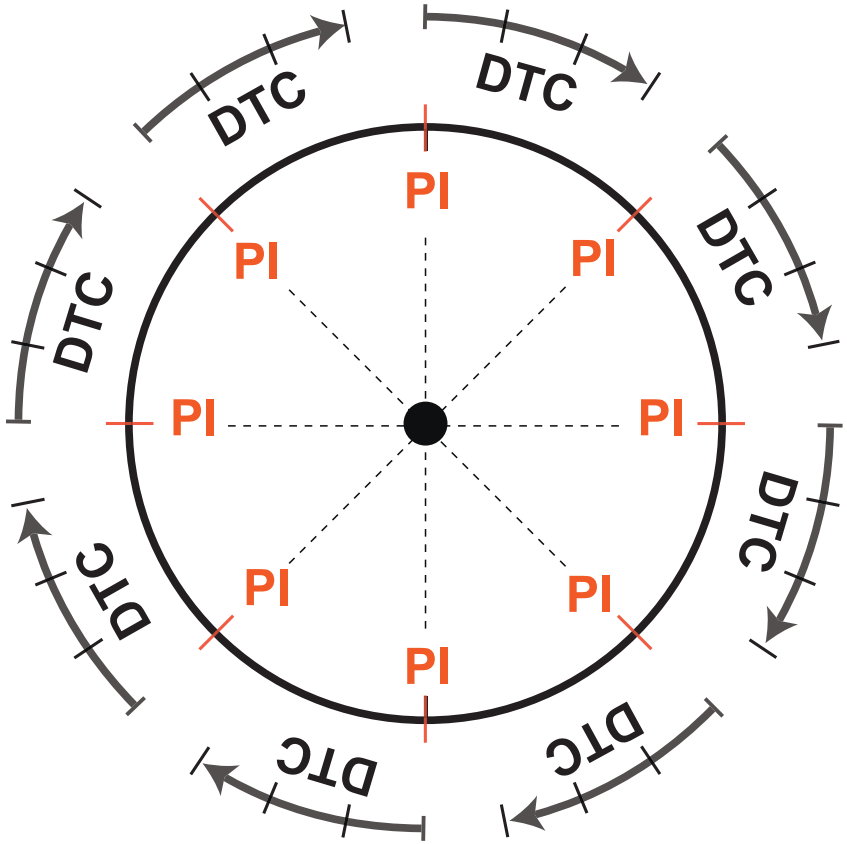
Error in threshold-crossing

$$\sigma^2_{\tau_{\mathrm{DR}}} = \frac{4\mathrm{kT}\gamma\,\tau_{\mathrm{DR}}}{I_n(V_{\mathrm{DD}} - V_{\mathrm{th}})}$$

Required dynamic range(dr)

$$\tau_{\mathrm{DR,DTC}} \geq \tau_{\mathrm{VCO}}$$

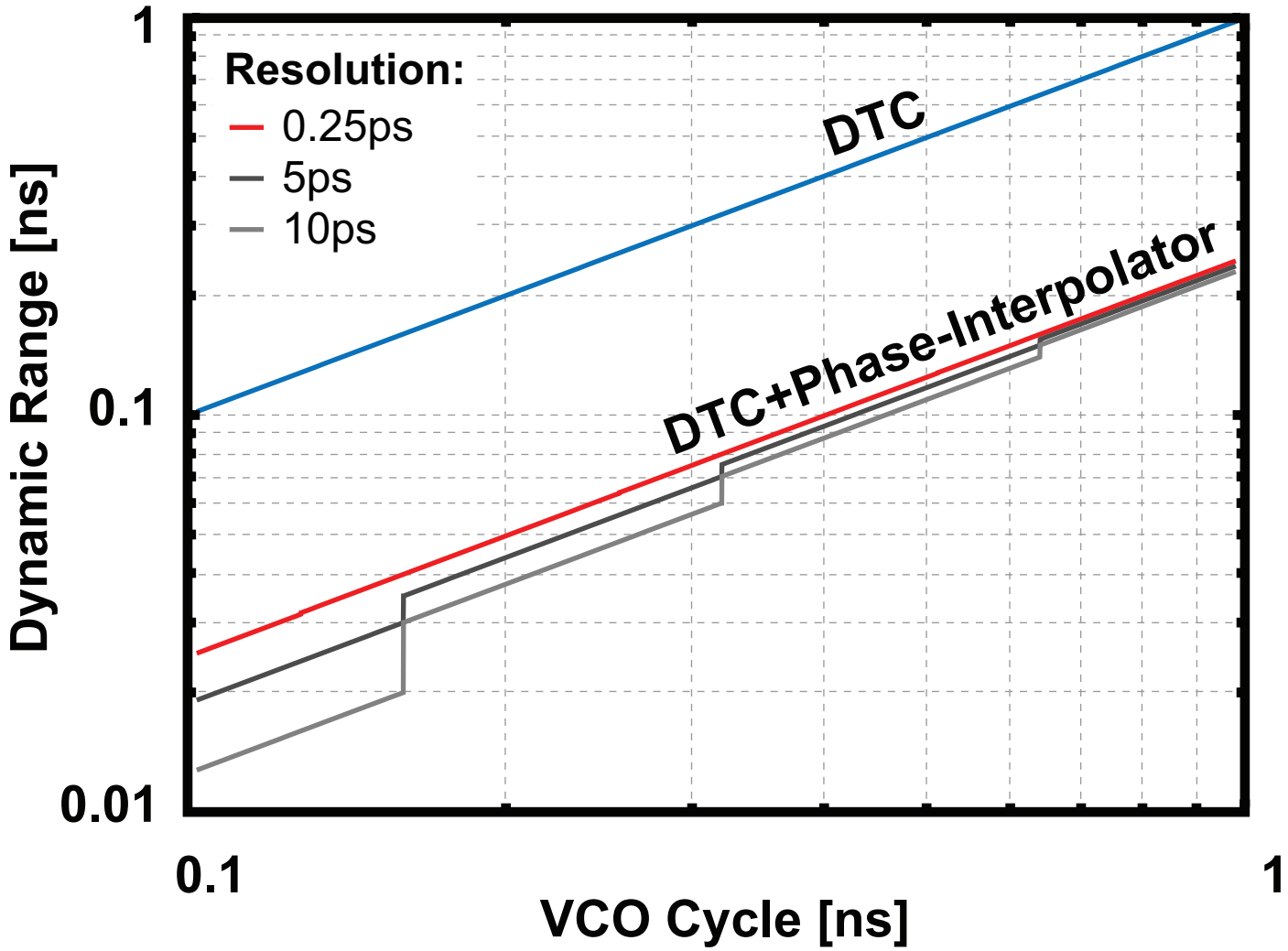
$$\tau_{\mathrm{DR,DTC+PI}} = \left[\frac{\tau_{\mathrm{VCO}}}{4}\sum_{i=1}^{N\_PI}\frac{1}{2^i}\right] + [\,\tau_{\mathrm{res}} \cdot (2^{N\_DTC} - 1)]$$



Phase Interpolator+DTC

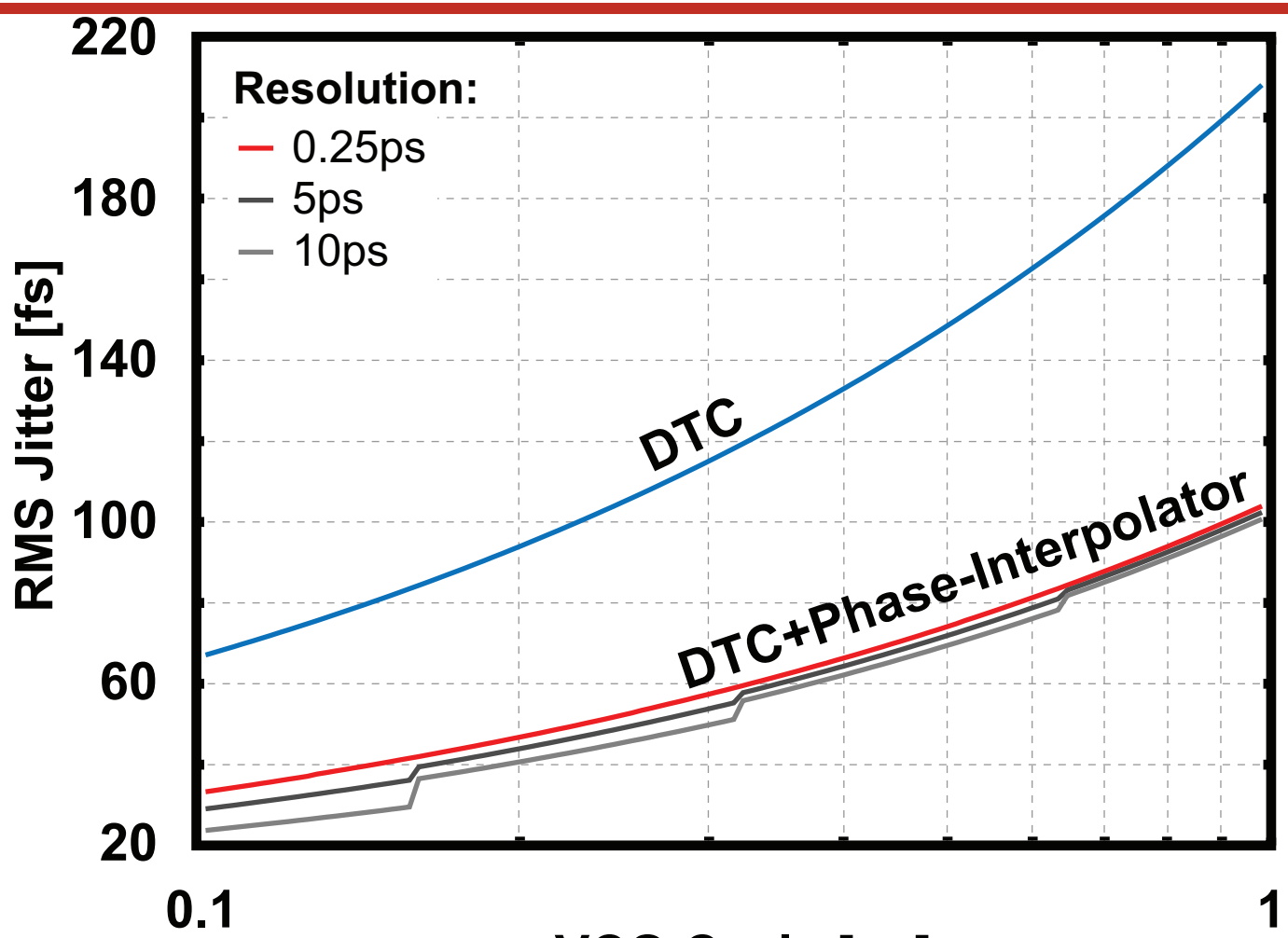
Highly linear phase-interpolator + DTC results in lower noise

Dynamic Range Comparison



Dynamic range requirements are relaxed

Intrinsic Jitter Comparison

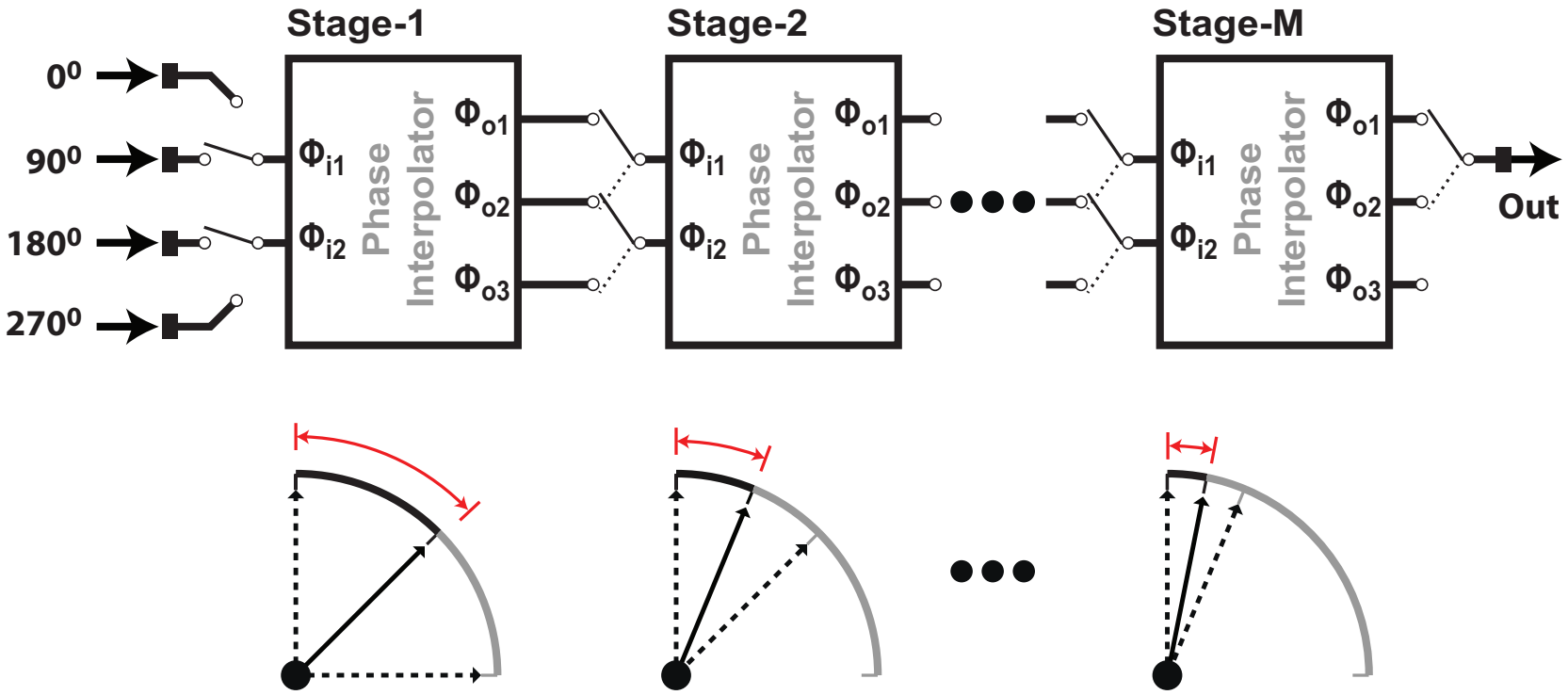


eg: Fvco = 4GHz, required resolution=250fs, DSM: second order

RMS Jitter: DTC only = ~150fs DTC+PI = ~50fs

Pipelined Phase-Interpolator

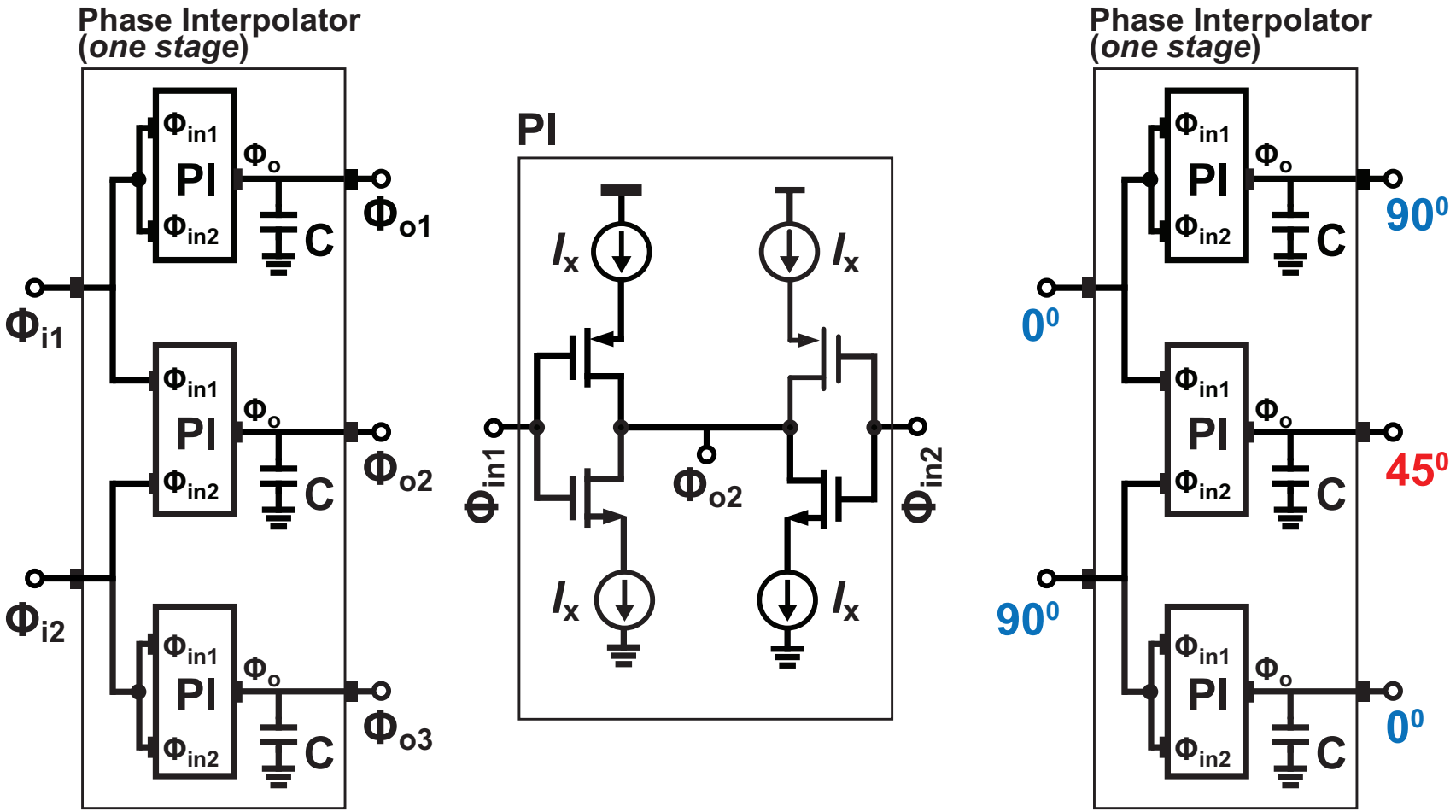
- No. of stages: Tournament type: $2^{N\_PI} - 1$
- No. of stages: Pipelined: N_PI+1



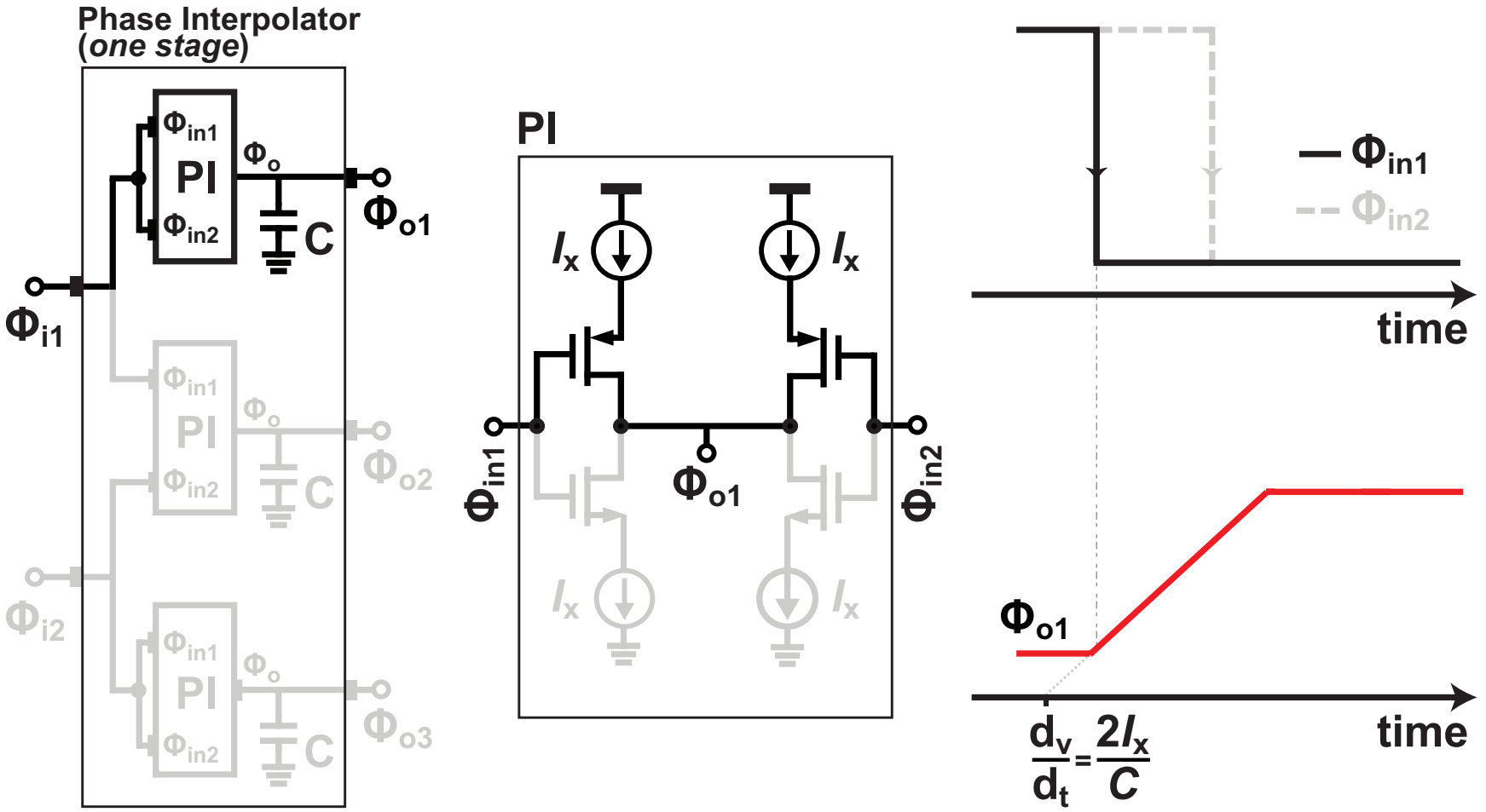
[5] S. Kumaki, APCCAS 2010

Power and area wastage is minimized

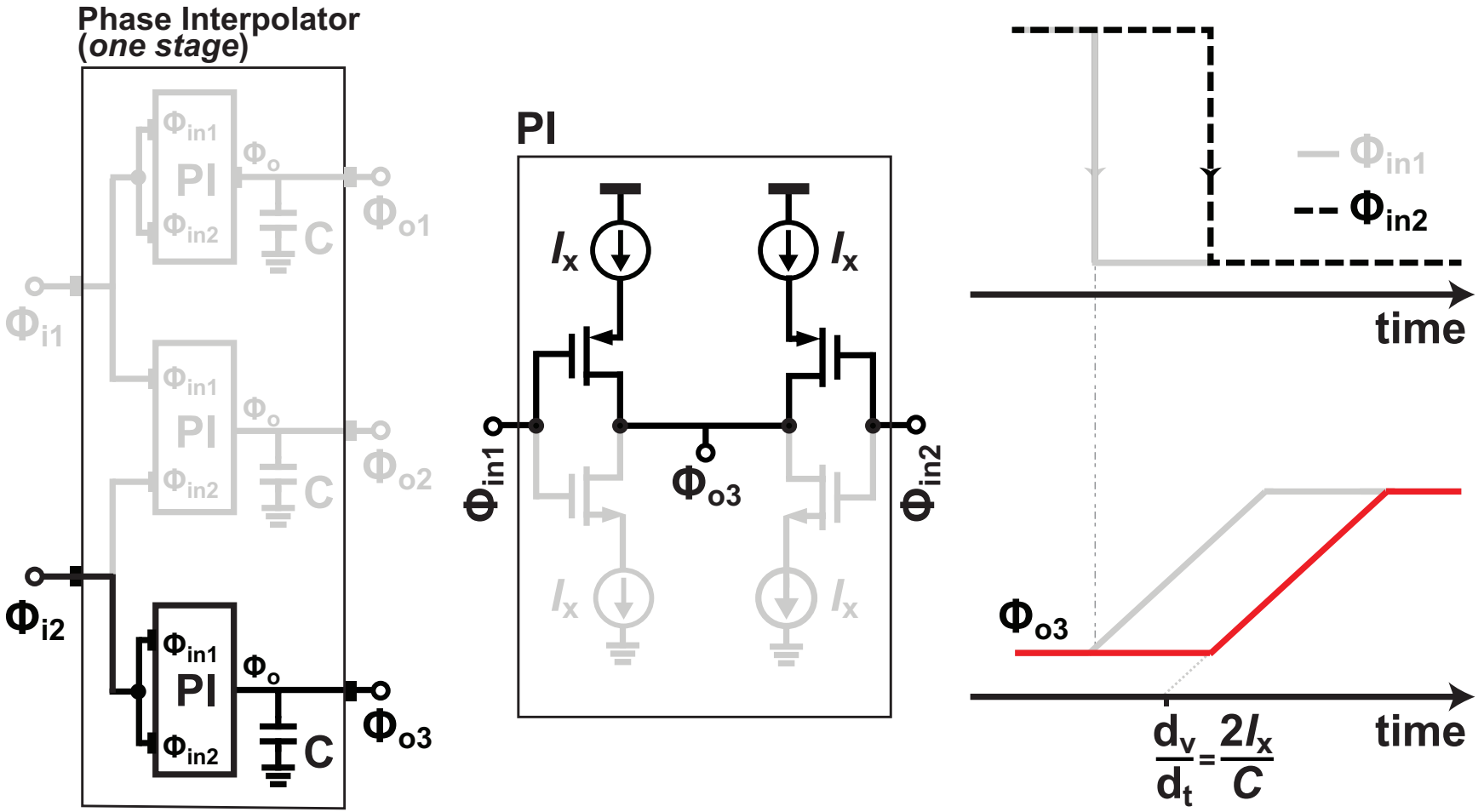
Issue of Conventional Phase-Interpolator



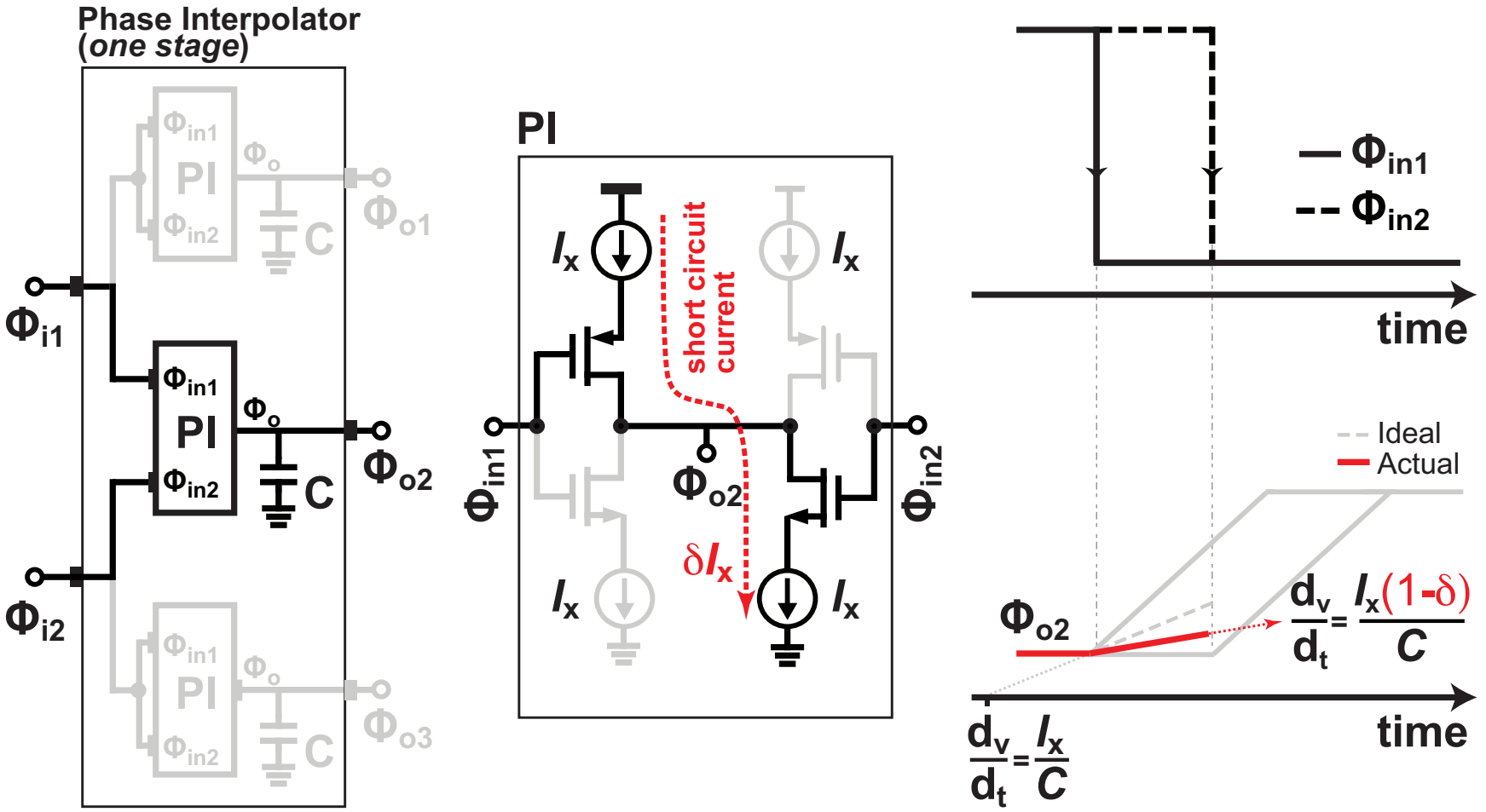
Conventional Phase-Interpolator



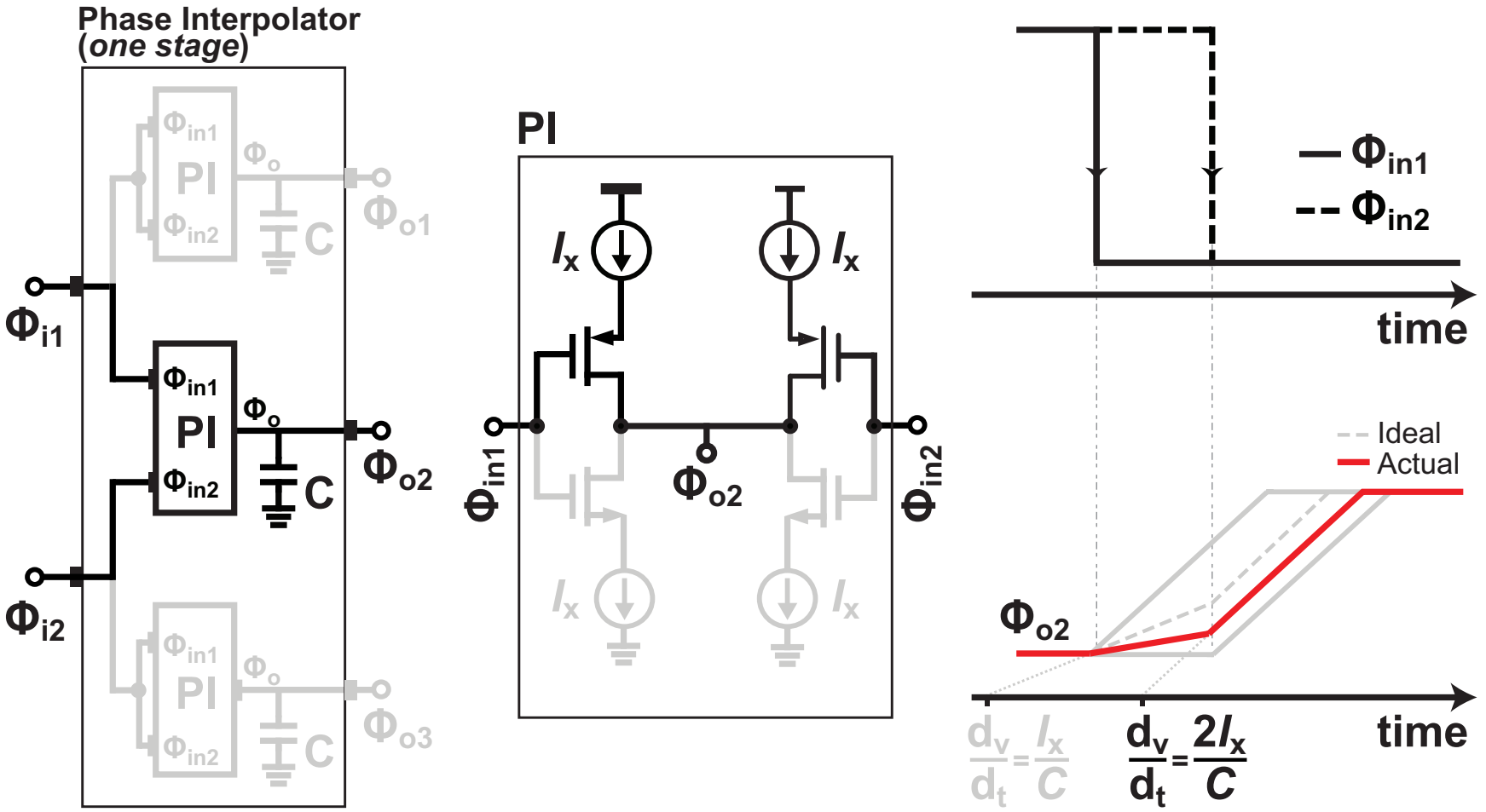
Conventional Phase-Interpolator



Conventional Phase-Interpolator

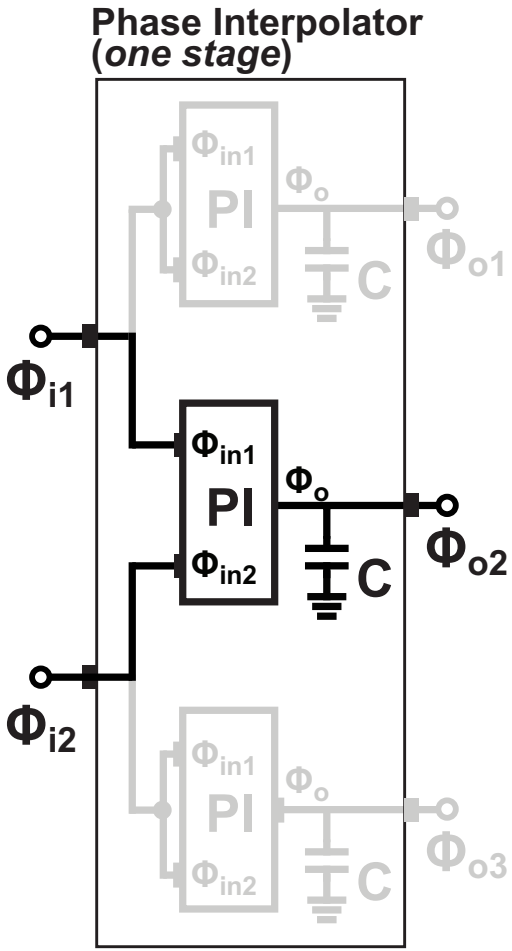


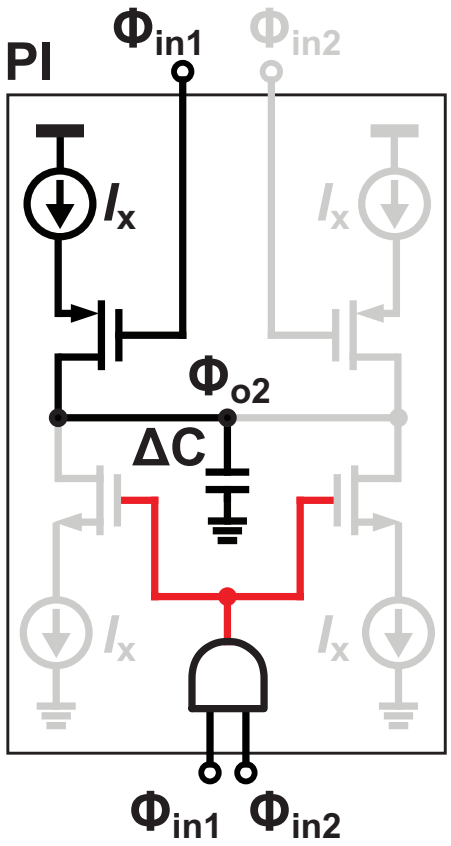
Conventional Phase-Interpolator

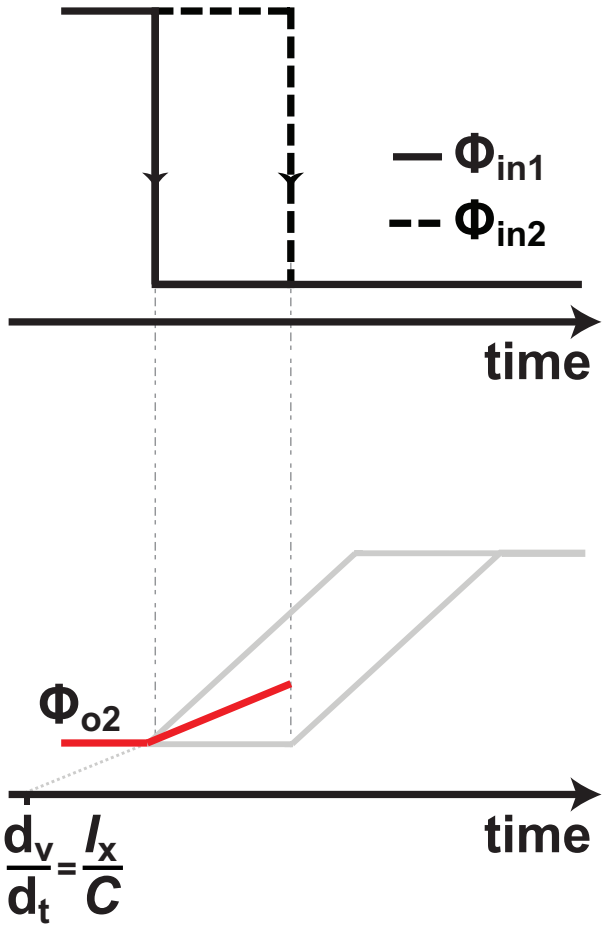


Short circuit current results in phase error

Proposed Short-Current-Free Topology

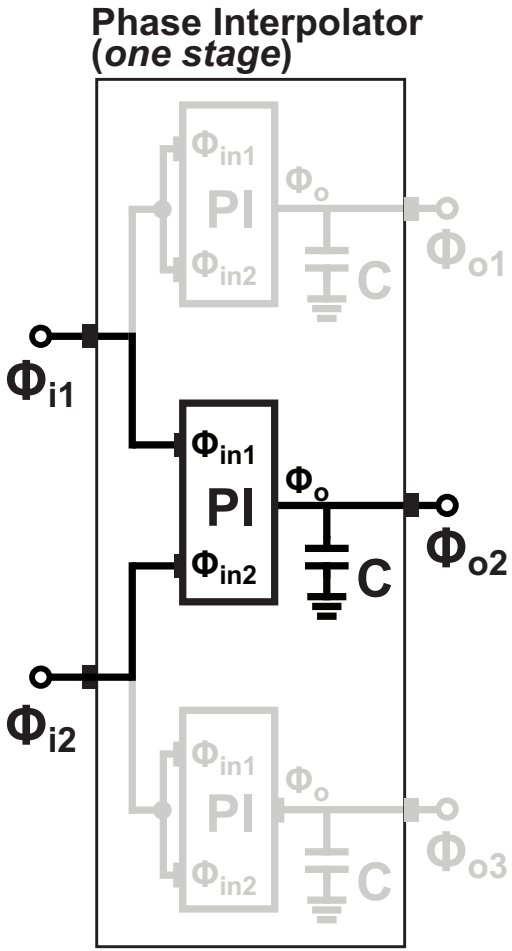


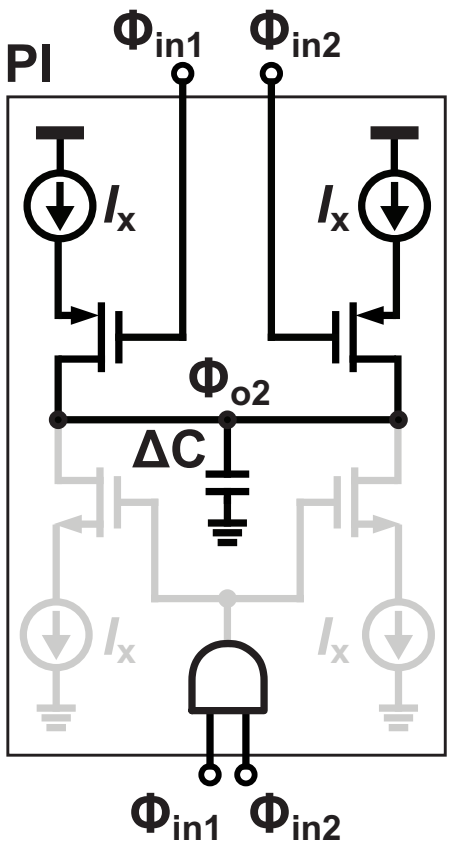


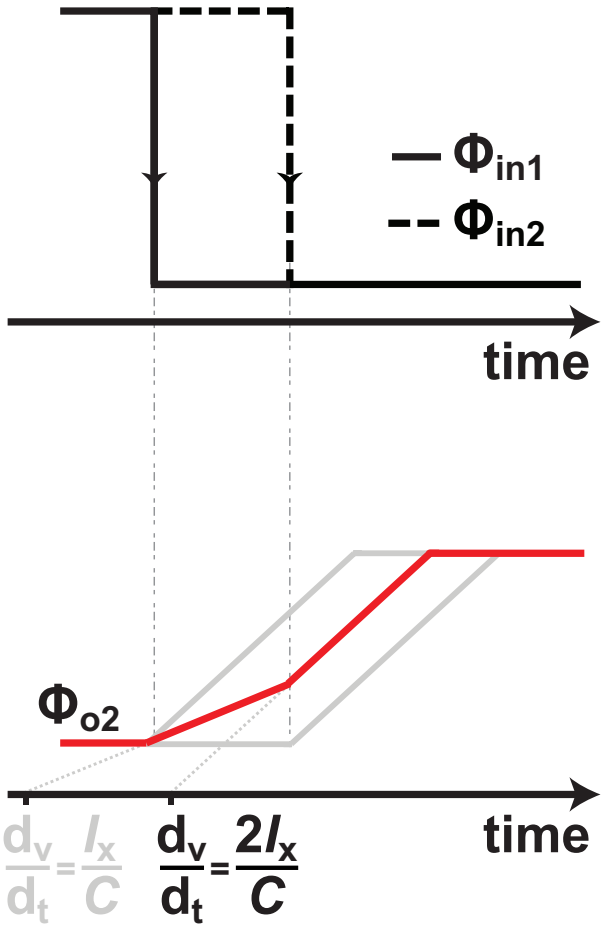


Short-circuit current is avoided

Proposed Short-Current-Free Topology



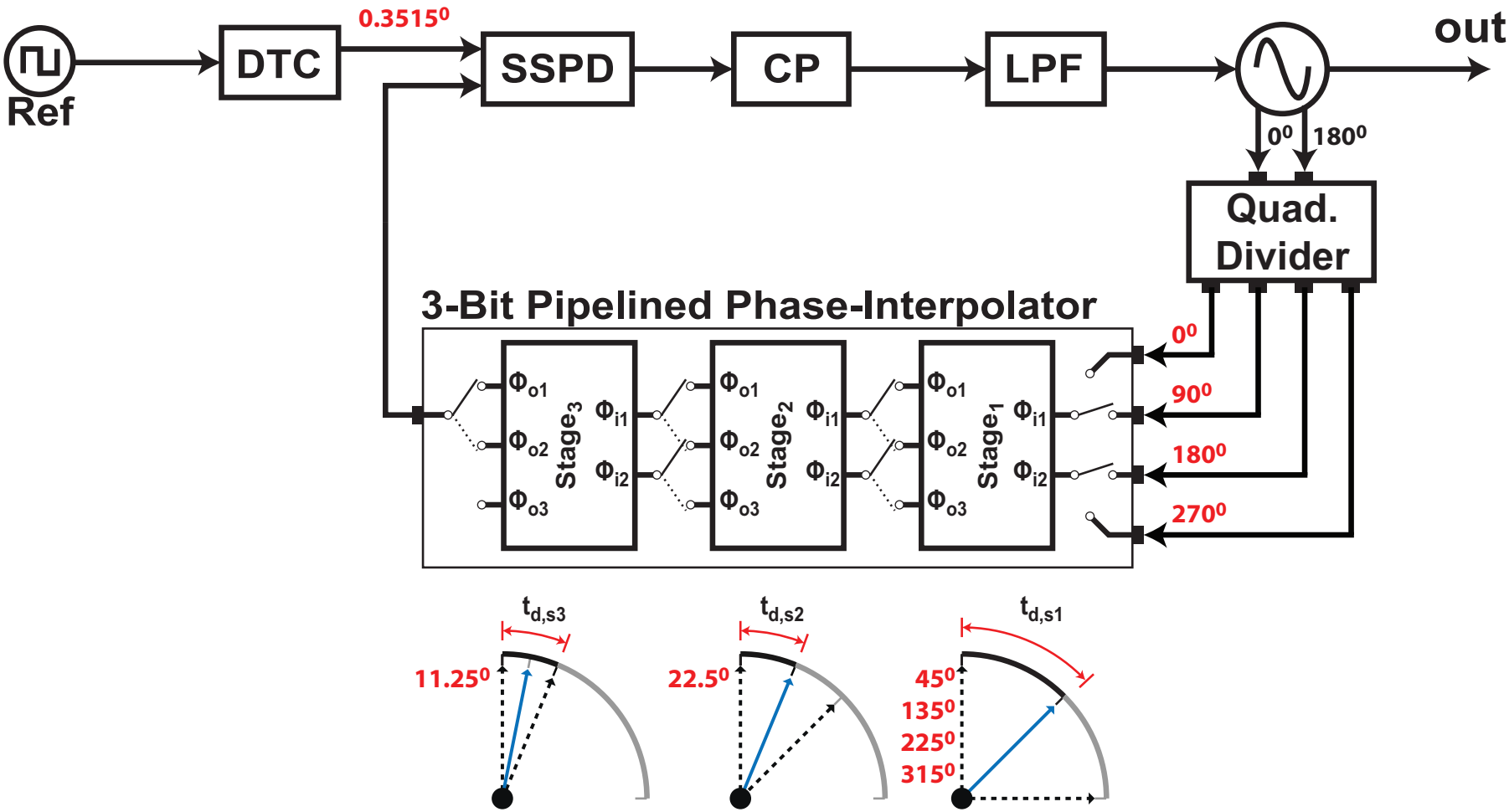




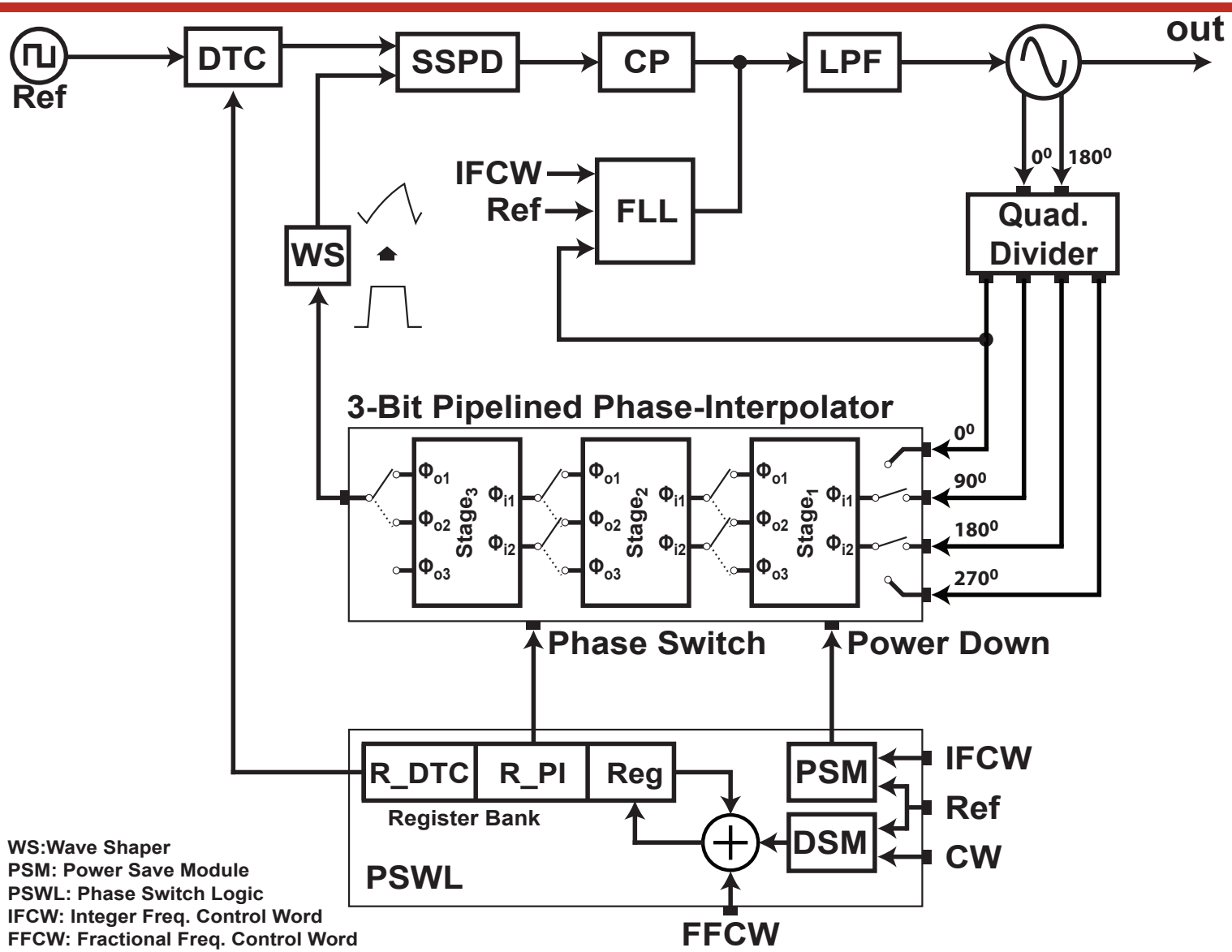
[6] T. Saeki, JSSC 2000

INL of < 0.5 LSB is achieved

Proposed FN-SSPLL Architecture

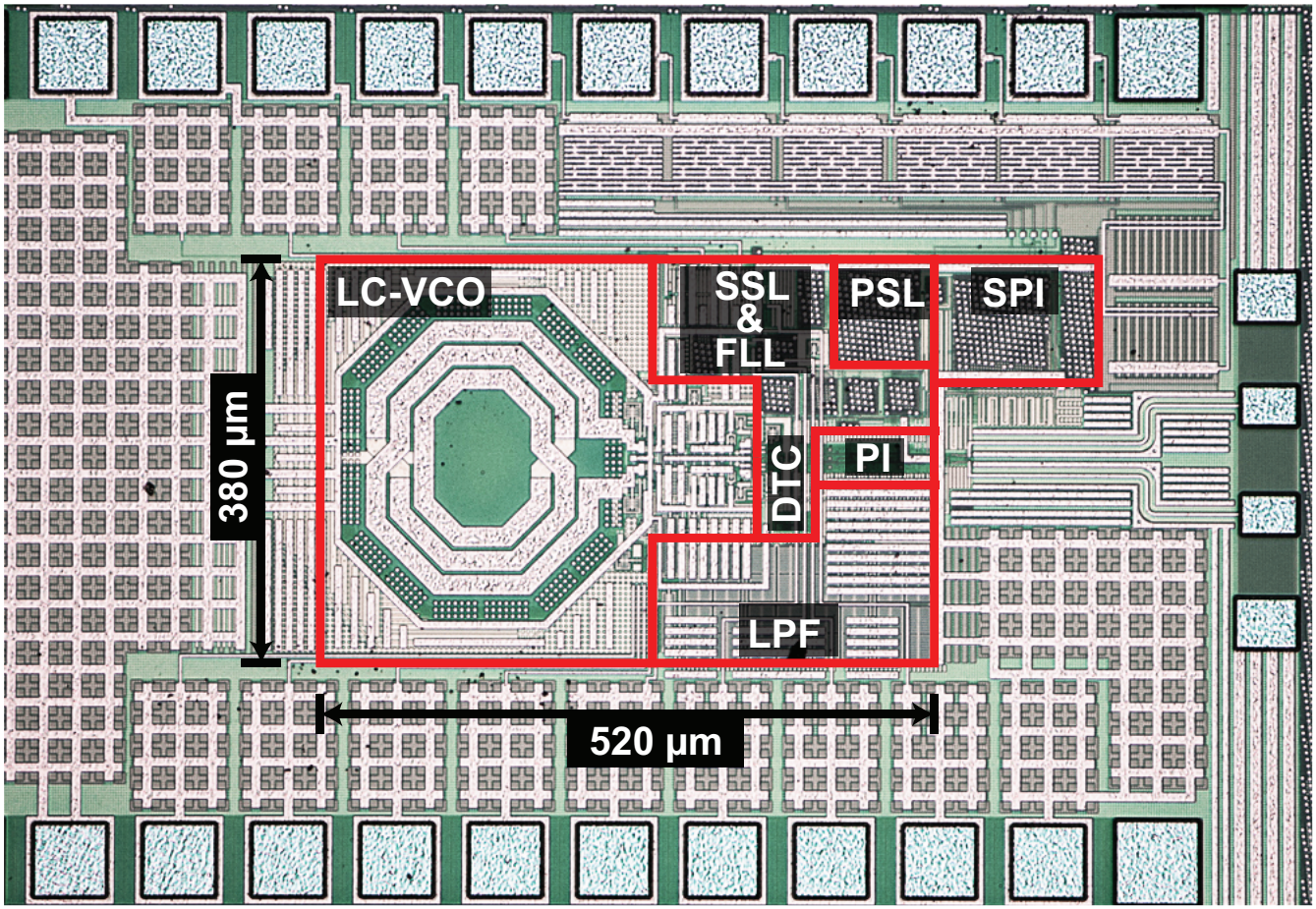


Proposed FN-SSPLL Architecture



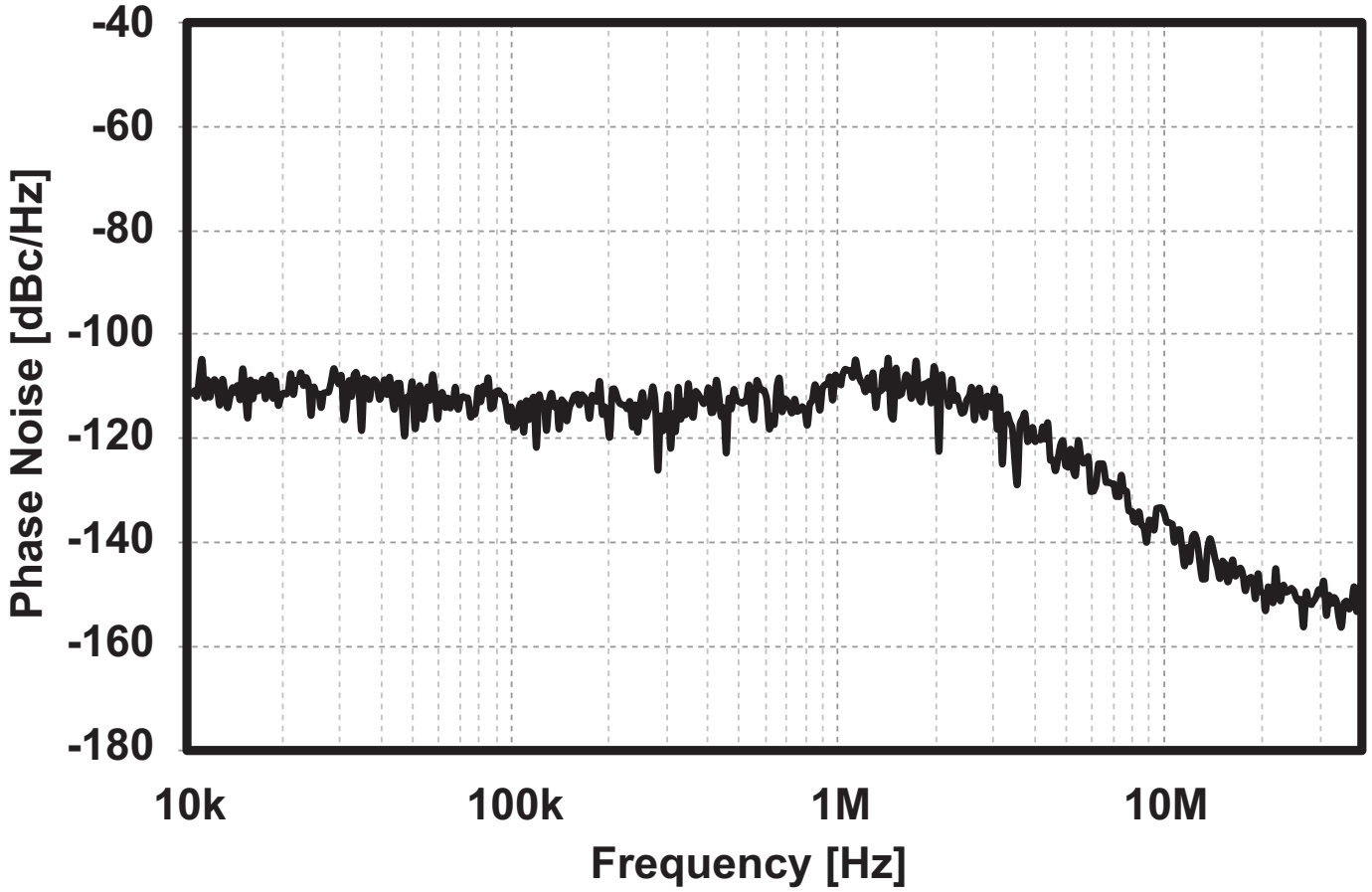
WS:Wave Shaper
PSM: Power Save Module
PSWL: Phase Switch Logic
IFCW: Integer Freq. Control Word
FFCW: Fractional Freq. Control Word

Chip Micrograph



0.2mm^2 core area in Standard 65nm CMOS process

Measurement Results



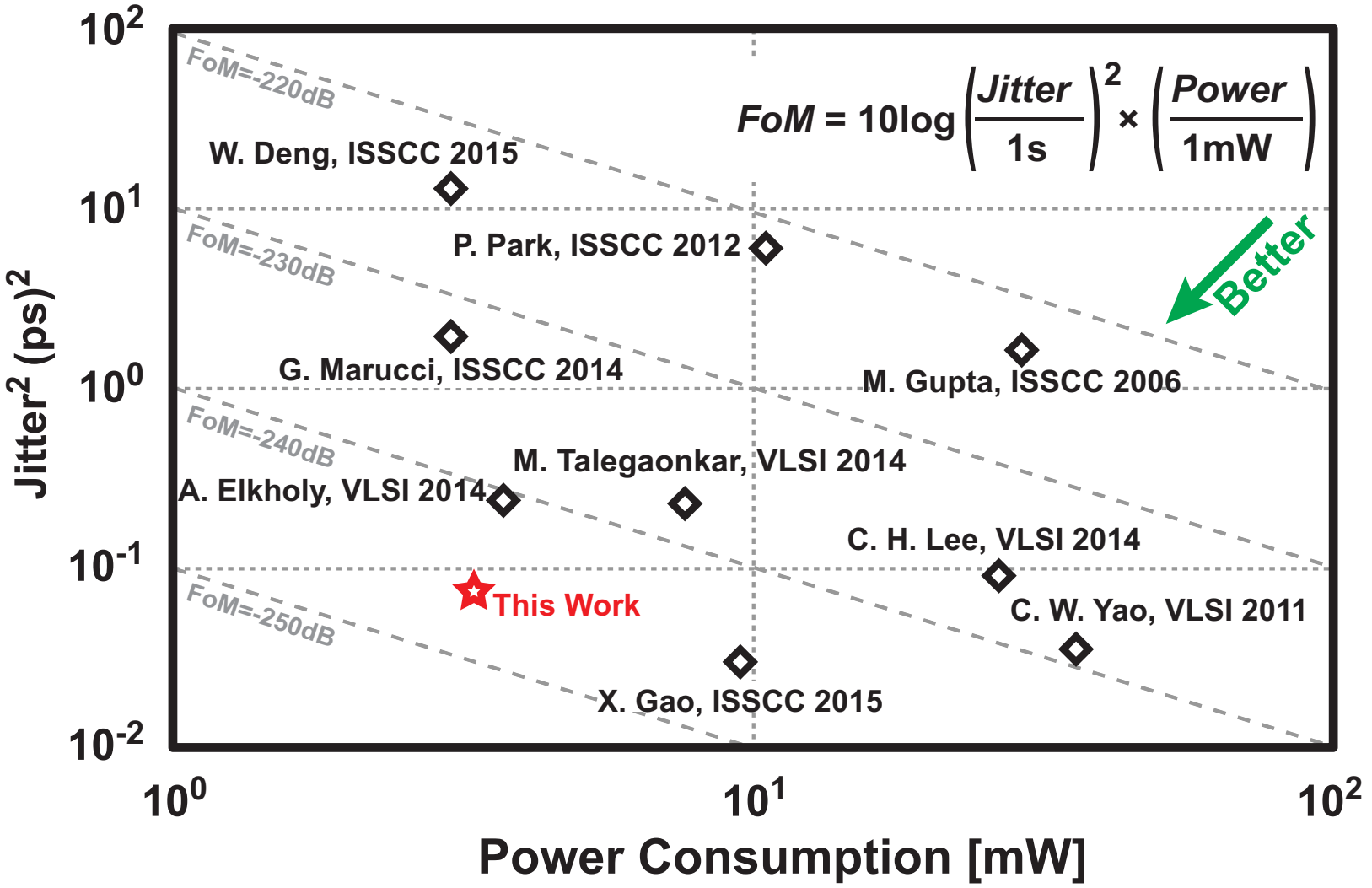
4.4716GHz from 40MHz reference [N=111.79]

Performance Comparison of Fractional-*N* PLL

	This work	[1]	[2]	[7]
Architecture	SSPLL	SSPLL	MDLL	TDC
Freq. [GHz]	4.1-5.1	2.2-2.4	1.6-1.9	2.412-2.484 4.915-5.825
Power [mW]	3.3	17.3	3	9.5
Area [mm^2]	0.2	0.75	0.4	0.3
Phase Noise (in-band)	-112 @400kHz	-112 @50kHz	-112 @100kHz	-106 @100kHz
Integrated Jitter	273fs	266fs	1.4ps	173fs
FoM [dB]	-246.1	-239.1	-233.76	-245.5
CMOS Tech.	65nm	180nm	130nm	28nm FDSOI

[1] Po-Chun Huang, ISSCC 2014 [2] G. Marucci, ISSCC 2014 [7] X. Gao, ISSCC 2015

Performance Comparison of Fractional-*N* PLL



Conclusion

- A fractional-*N* SSPLL architecture is presented.
- Proposed architecture uses a combination of DTC and phase-interpolator:
  - Reduces jitter from the multi-phase generator.
  - Power-jitter-resolution tradeoff is mitigated.
  - FoM of -246.1dB is achieved.

THANK YOU