A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs

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***Abstract* - This paper presents a low offset voltage, low noise dynamic latched comparator using a self-calibrating technique. The new calibration technique does not require any amplifiers for the offset voltage cancellation and quiescent current. It achieves low offset voltage of 1.69 mV at 1 sigma in low power consumption, while 13.7 mV is measured without calibration. Furthermore the proposed comparator requires only one phase clock while conventionally two phase clocks were required leading to relaxed clock. Moreover, a low input noise of 0.6 mV at 1 sigma, three times lower than the conventional one, is obtained. Prototype comparators are realized in 90 nm 10M1P CMOS technology. Experimental and simulated results show that the comparator achieves 1.69 mV offset at 250 MHz operating, while dissipating 40 μW/GHz (20 fJ/conv.) from a 1.0 V supply.**

I. Introduction

A high-speed, low-offset, low-power consumption comparator is very attractive for many applications, such as memory sensing circuits, analog to digital converters and data receivers. While the technology scaling of MOS transistors enables high-speed and low-power operation, the offset voltage of the comparator is increased due to the transistor mismatch. In conventional designs, pre-amplifiers are used to reduce offset voltage [1]. However, these techniques require high voltage gain to reduce the offset voltage and loosing effectiveness with the reduction of the drain resistance due to the technology scaling. Moreover, large power consumption of the amplifier is inevitable for realizing a wide bandwidth amplifier. On the other hand, a dynamic comparator which has the offset compensation function was proposed [2]. In this method the same input signal of each comparator as the reference voltage is given in flash type ADC, and the load capacitances of the output node of each comparator are controlled digitally so that the output of the comparator may reach the ideal value. However, the calibration time greatly increases if the resolution of the ADC is increased. Moreover, the speed of the comparator is slowed down due to the increase of added capacitances. Additionally, the considerably large size circuits to control the calibration are necessary for each comparator. Therefore this topology is improper for the design of high resolution flash type ADCs.

Moreover, a comparator noise determines the signal to noise ratio of ADCs. This is especially true for a high resolution successive approximation ADC which requires a sufficiently low noise comparator to prevent conversion errors [3].

In this paper, a dynamic latch type low noise comparator using self-calibrating technique is proposed. The proposed offset calibration technique does not require quiescent DC current for offset cancellation owing to use of a charge pump circuit instead of a pre-amplifier. Thus, the proposed offset cancellation achieves not only low offset voltage but also low power consumption. Moreover, the proposed circuit topology can improve the comparator noise and reduce the clock driving requirement compared with a conventional comparator.

II. Circuit Design

A. Self-Calibrating Technique

The calibration architecture for the offset voltage cancellation of the comparator is shown Fig. 1. The proposed architecture consists of a comparator, offset compensation current sources (M_C1, M_C2) and a charge pump. During the calibration mode, all input nodes of the comparator are switched from the signal inputs to the common-mode voltage V_{cm}.

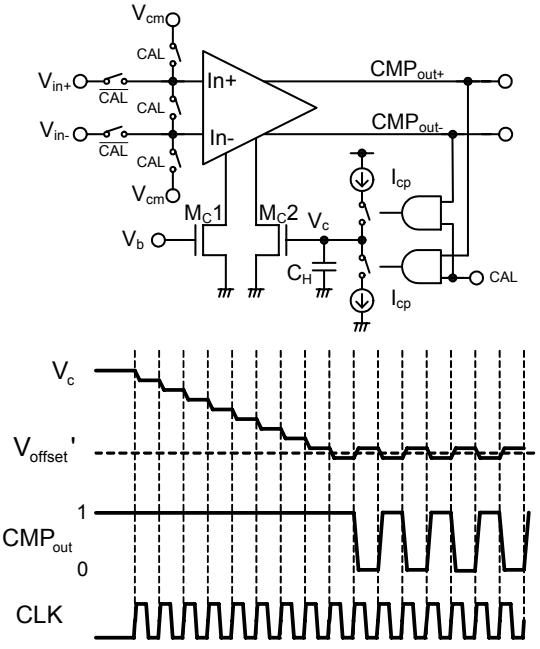
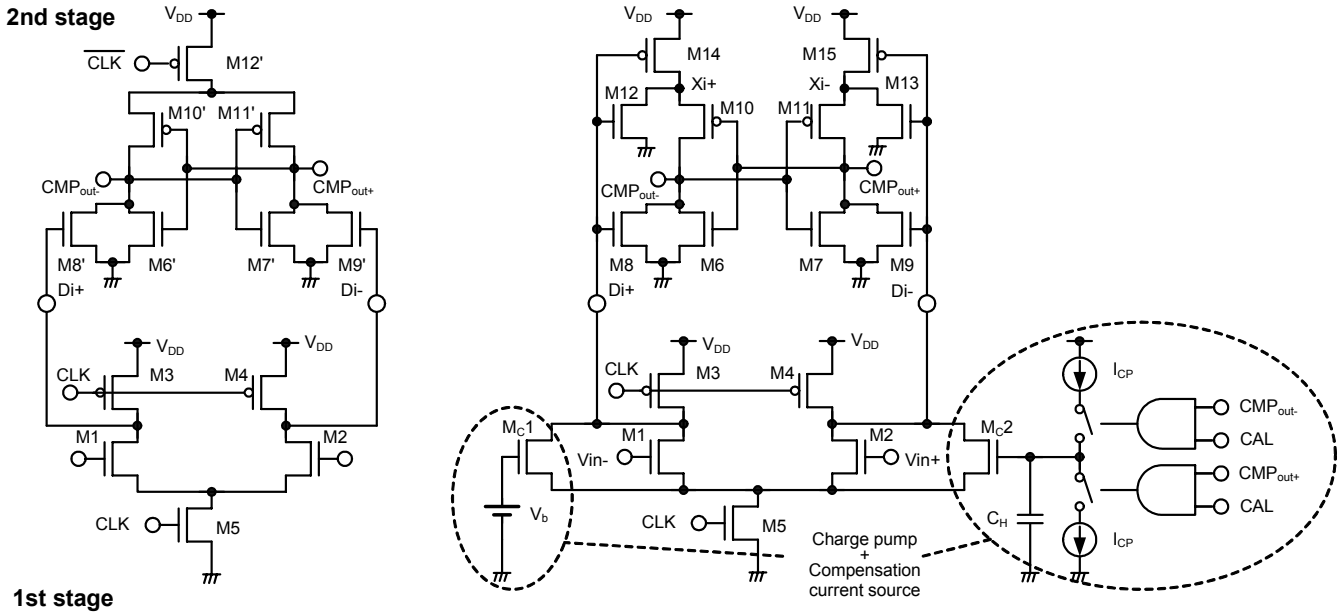


Fig. 1. Proposed calibration architecture for offset cancellation.



(a) Conventional comparator

(b) Proposed self-calibrating comparator

Fig. 2. Circuit Implementation.

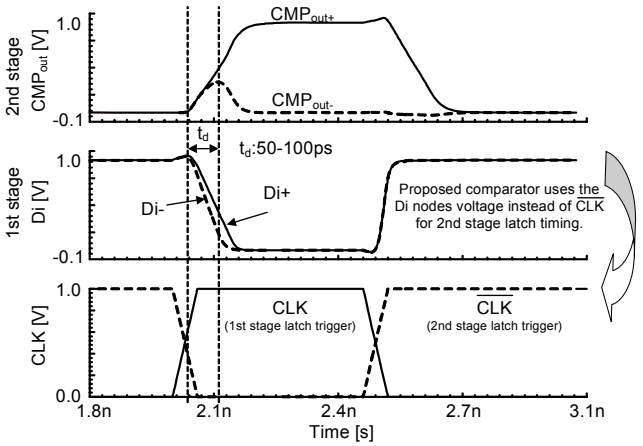


Fig. 3. Signal behavior of the conventional and proposed comparators.

Transistors M_C1 and M_C2 used to generate the compensation current are connected to the internal output node of the comparator. The gate of M_C1 is connected to V_b to set the common mode voltage of the charge pump.

The gate of M_C2 is connected to the capacitor C_H which is pre-charged to V_b in the initial condition. If the comparator has the offset voltage V_{offset} (V_{offset} is positive value in this case) the comparator outputs high, and pulls out the charge of C_H according to the current I_{cp}, along with the control voltage of the current source V_c falls, causing the offset voltage of the comparator approaches zero. When V_c exceeds V_{offset}' corresponding to the offset of the comparator being adjusted to zero, comparator outputs high and low alternately as shown in Fig. 1. During the conversion mode, C_H keeps the offset value. Thus, the offset voltage is canceled in conversion mode.

The comparator offset voltage becomes less than ±1 LSB ($= T_s \times I_{cp} / C_H$) due to the charge pump if the comparator has no hysteresis characteristics or noise. A wide compensation range can be realized by changing I_{cp}. The proposed calibration technique does not require a reference voltage for the calibration. Because each comparator can calibrate for the offset simultaneously, the calibration time can be remarkably shortened in a system that needs a lot of comparators, such as flash type ADCs. The circuit can be made simple and the die area also can be reduced because the input of the calibration data word from outside of the comparators is not required. In practice, offset voltage cancellation is limited by sensitivity of the comparator. Therefore a low noise comparator is needed for achieving low offset voltage in the proposed architecture.

B. Circuit Implementation

The conventional comparator and our proposed circuit are shown in Fig. 2. The signal behavior of these comparators is shown in Fig. 3.

The proposed circuit consists of a comparator based on a double latch type comparator [4] (M1-15), compensation current source (M_C1-2) and charge pump circuit.

During the reset phase (CLK = 0), M3 and M4 pre-charge the D_i nodes to supply voltage V_{DD}. This result in, M8 (M8') and M9 (M9') discharging the output nodes to ground. After reset phase, CLK turns to V_{DD}, M3 and M4 turn off and M5 turns on. At the D_i nodes, the common-mode voltage drops with a rate determined by I_{M5} / C_{Di} (C_{Di} is the load capacitance of the 1st stage) and an input dependent differential voltage ΔV_{Di} will build up in a short time. The conventional comparator requires high accuracy timing $\overline{\text{CLK}}$ because the second latch stage has to detect ΔV_{Di} at very short time t_d.

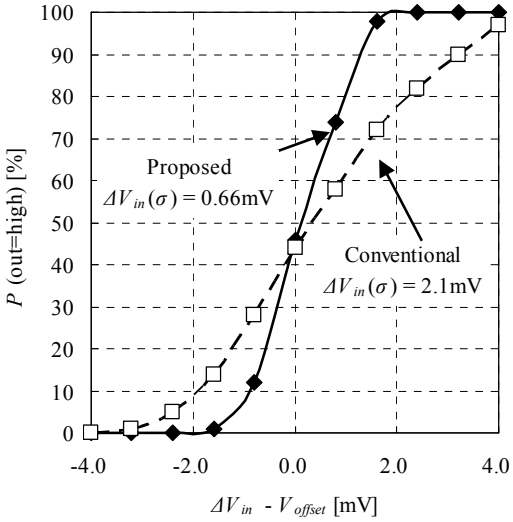


Fig. 4. Simulated cumulative noise distribution.

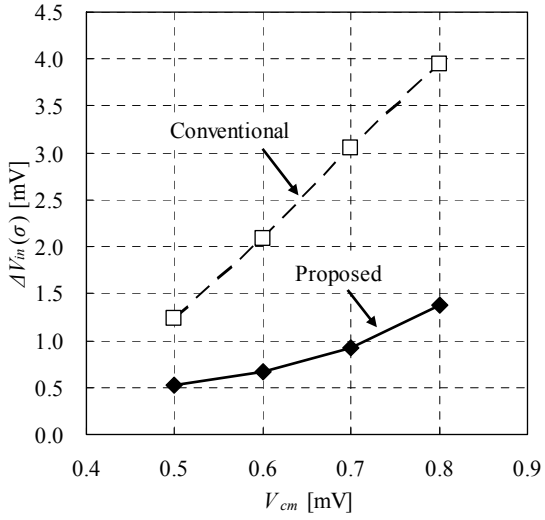


Fig. 5. Simulated equivalent input noise $\Delta V_{in}(\sigma)$ obtained from cumulative noise distribution vs. common mode input voltage.

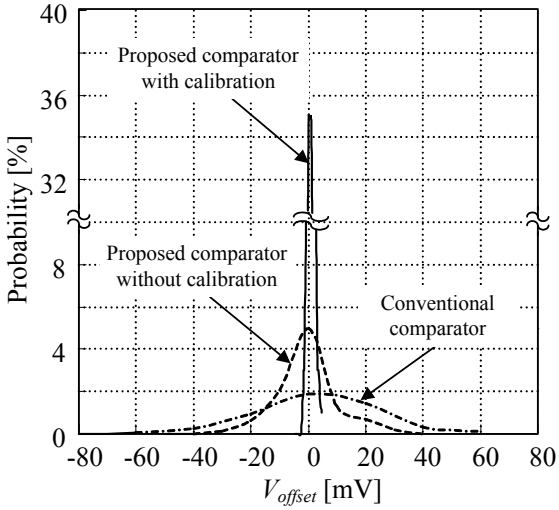


Fig.6. Simulated distribution of the input offset voltage V_{offset}.

TABLE I
SIMULATED INPUT OFFSET VOLTAGE

Simulation condition	$V_{offset}(\sigma)$
Conventional comparator	21.5 mV
Proposed comparator without calibration	13.5 mV
Proposed comparator with calibration	1.3 mV

The proposed comparator uses the falling edge at the D_i nodes for the latch timing of the second stage. M14 and M15 are used instead of M12' and these gates are connected to the D_i nodes. M14 and M15 behave not only pre-charge switches but also input transistors of the second latch stage. Therefore, the comparator sensitivity is improved by increasing the gain of the second latch stage. Moreover, the clock driving requirements are relaxed because the proposed comparator requires only a one phase clock. M12 and M13 are used to reset the X_i nodes to avoid mismatch voltage between X_i nodes that causes comparator offset.

Fig. 4 shows the simulation results of the comparator noise obtained with *Spectre* transient noise simulation. The operating conditions are V_{DD} = 1.0 V, clock frequency f_{CLK} = 4 GHz and the common-mode voltage of the comparator input V_{cm} = 0.6 V. Same size transistors are used in the conventional and the proposed comparator. The offset cancellation was disabled in this simulation. Fitting the simulation results to a Gaussian cumulative distribution gives the RMS equivalent input noise $\Delta V_{in}(\sigma)$. $\Delta V_{in}(\sigma)$ in the proposed comparator equals 0.66 mV and while conventional one equals 2.1 mV. The simulation result shows the noise of the proposed comparator is about 3 times lower than the conventional one. Fig. 5 shows the simulated equivalent input noise $\Delta V_{in}(\sigma)$ obtained from cumulative noise distribution versus common mode input voltage V_{cm}. $\Delta V_{in}(\sigma)$ of the proposed circuit increases by only 1.0 mV when V_{cm} changes from 0.5 V to 0.8 V, in contrast to the 2.8 mV increase for the conventional comparator.

The offset voltage obtained from simulation is shown in Fig. 6 and Table I. The simulation result of the proposed comparator on 100 samples gave an offset voltage distribution of $V_{offset}(\sigma)$ = 13.5 mV versus 21.5 mV in the conventional comparator when calibration technique is not used. The offset voltage is improved by increasing the trans-conductance of the input transistors in the second stage. The offset voltage distribution can be improved to 1.3 mV, when calibration is enabled.

III. Measurement Results

A prototype comparator has been realized in a 90 nm 10M1P CMOS technology with a chip area of 0.0348 mm^2 as shown in Fig. 7. The chip area includes 64 comparators with SR latches to create a static output.

The offset voltage of the comparator with and without calibration is shown in Fig. 8. The offset voltage is measured on 64 samples, V_{DD} = 1.0 V and f_{CLK} = 250 MHz. The offset calibration had been executed before the offset voltage

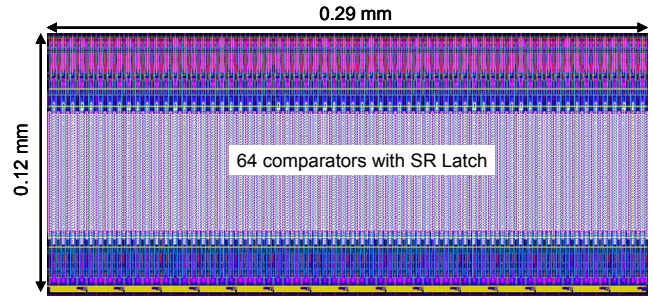


Fig. 7. Layout of the proposed comparator.

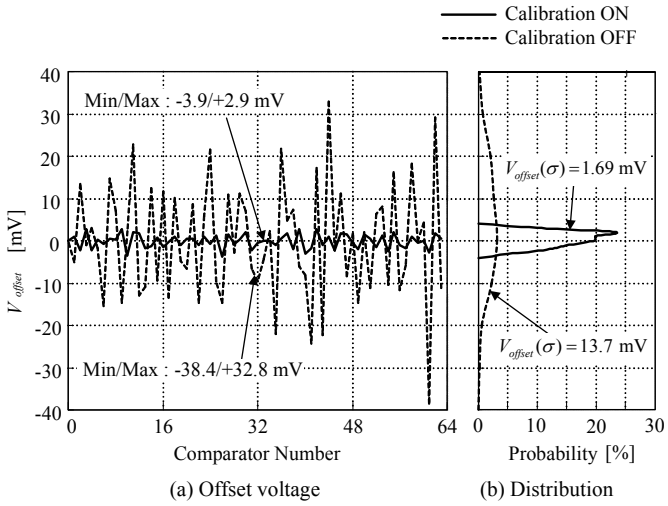


Fig. 8. Measured offset voltage of the comparator with and without calibration.

measurement.

Measurement results show that the offset voltage is dramatically improved from 13.7 mV to 1.69mV by using the proposed calibration architecture.

Fig. 9 shows the measured input noise $\Delta V_{in}(\sigma)$ versus common mode input voltage. The input noise is measured on V_{DD} = 1.0 V and V_b = 0 V. The offset cancellation is disabled in this measurement. Measurement results show that the comparator noise is decreased by the decrease of V_{cm}. $\Delta V_{in}(\sigma)$ increases by only 0.16 mV when f_{CLK} is changed from 200 MHz to 600 MHz.

The delay time of the comparator (the time is defined by the time between the clock edge and the instant when CMP_{out} crosses 70 % of V_{DD}) obtained from the simulation is 122 ps at 1mV input voltage difference and delay / log(ΔV_{in}) is equal to -24.3 ps/dec. The simulated power consumption of proposed comparator is 40 μW, the FoM amounts to 20 fJ/conv. at a conversion frequency of 1 GHz with a supply-voltage of 1.0 V.

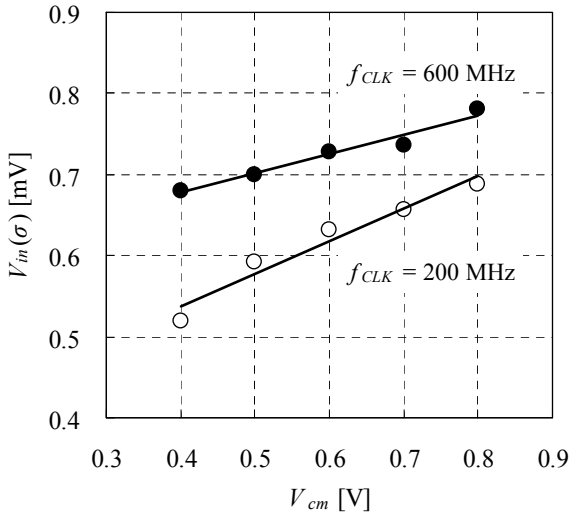


Fig. 9. Measured equivalent input noise $\Delta V_{in}(\sigma)$ vs. common mode input voltage V_{cm}.

IV. Conclusion

A low-offset, low-noise dynamic latched comparator using a self-calibrating architecture that does not require a preamplifier and a DAC is proposed. Measured results show the RMS input offset voltage is dramatically improved from 13.7 mV to 1.69 mV by using proposed calibration technique. The comparator noise is only 0.6 mV in case of V_{cm} = 0.5 and f_{CLK} = 200 MHz and 0.7 mV in case of V_{cm} = 0.5 and f_{CLK} = 600 MHz. This value is three times lower than that of the conventional one.

The proposed comparator can compare 1.0 mV input voltage at 1 GHz with a low power consumption of 40 μW/GHz (20 fJ/conv.). The proposed calibration technique and comparator topology are very effective for achieving a small area and low offset voltage comparator using a deep sub-micron CMOS technology.

Acknowledgement

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References

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