SAR+ΔΣADC with Open-Loop Integrator using Dynamic Amplifier

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Background and Motivation

Design concepts
• ADC architecture
• Open-loop integrator
• Dynamic amplifier
• Binary-mode DEM

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SAR+DS ADC for CMOS image sensor

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Background

- **SAR ADCs**
  - ☀ Lowest power consumption with clock scalability
  - ☹ SNR is limited by noises (Comp., Ref., mismatch)

- **ΔΣ ADCs**
  - ☀ Highest SNR
  - ☹ Power consuming of an Opamp in an integrator

- **Noise-shaping SAR ADCs [1, 2]**
  - ☀ High SNR and high efficiency
  - ☹ Opamps are still used

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Previous works 1

Switched Opamp [3]

Overhead of the recovery time

Opamp average current = \frac{\text{Recovery time} + \text{Operating time}}{\text{ADC conversion period}} I_{\text{bias}}

Fully passive integrator [4]

_low gain, incomplete integration => Only for low OSR_

\[ Y = X + \frac{(0.5z^{-1} - 1)(1 - 0.6z^{-1})}{1 + 0.2z^{-1}} \frac{V_{res, plus}(z)}{0.5} \]

Previous works 3

Passive integrator with dynamic pre-amp [5]

Higher gain, but incomplete integration

\[
D_{\text{out}}(z) = V_{\text{in}}(z) + \frac{1 - 0.8z^{-1}}{1 + 1.2z^{-1} + 0.667z^{-2}} Q(z)
\]

An incomplete integrator cannot suppress $Q_n$ at low freq.

**Ex.)** @ $F_{in} = 1/20$
- Ideal = -32.2 dB
Our Design Concepts

Open-loop Integrator

• A complete integrator can be realized by using a low gain open loop amplifier and switched capacitors
• Dynamic amplifiers achieve low power consumption and clock scalability

Binary-mode DEM

• Simple structure
• Low power and small area
Target SQNR

Target SQNR > 95dB
SAR ADC part : 6bit, SQNR = 38dB
DSM part : $Q_n$ suppression > 57dB @OSR=20

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ADC Architecture

![Diagram of ADC Architecture]

- **SAR Conversion Integration**
- **Reset**
- **Sampling**
- **Integration**

- 6bit CDAC
- Binary-mode DEM
- SAR Logic
- $V_{in}$
- $D_{out}$ 6bit

G1 = 0.5, G2 = 0.33, G3 = 0.33

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Proposed Open-loop Integrator

Conventional closed-loop integrator

Phase: $\phi_1$

$V_{out} = V_{out_{n-1}}$

Proposed open-loop integrator

Phase: $\phi_1$

$V_{out} = V_{out_{n-1}}$

$V_1 = A_1 V_{in}$

$V_2 = A_2 V_{out_{n-1}}$
Proposed Open-loop Integrator

Proposed method can realize a complete integration

Conventional closed-loop integrator

Proposed open-loop integrator

V_{out} = V_{out_{n-1}}

Phase: \( \phi_1 \)

V_{out} = V_{out_{n-1}} + V_{in}

Phase: \( \phi_2 \)

\( A_1 = 3, \ A_2 = 2, \)

V_{out} = (V_{out_{n-1}} + V_1 + V_2)/3

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Dynamic Amplifier Design

- No DC current
- Gain controllable $1.5x \sim 4.5x$, 5bit resolution
Open loop vs. Closed loop

An open loop integrator achieves 50~90% power reduction

![Graph showing open loop vs. closed loop performance]

<table>
<thead>
<tr>
<th></th>
<th>Proposed</th>
<th>Opamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain (V/V)</td>
<td>3</td>
<td>100</td>
</tr>
<tr>
<td># of unit</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Integrator Type</td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>Integrator Output noise</td>
<td>100μV RMS</td>
<td></td>
</tr>
<tr>
<td>Settling error</td>
<td>-</td>
<td>1%</td>
</tr>
<tr>
<td>Settling time</td>
<td>1.8ns</td>
<td></td>
</tr>
<tr>
<td>Clock Freq.</td>
<td>150MHz</td>
<td></td>
</tr>
<tr>
<td>Recovery time</td>
<td>None</td>
<td>1 CLK (6.7ns)</td>
</tr>
</tbody>
</table>
Gain error influence

Gain error of $\pm 20\%$ can be accepted ($|\Delta \text{SNDR}| < 3\text{dB}$)

Simulated SNDR vs. gain error of amplifier used in 1st integrator

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ADC Architecture

Binary-mode DEM

6bit CDAC

DSM

SAR Logic

V_{in}

D_{out}

6bit

G_1=0.5, G_2=0.33, G_3=0.33

Reset Sampling SAR Conversion Integration

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Randomly select left(0) or right(1) unit capacitors in each conversion.

3bit example

<table>
<thead>
<tr>
<th>DEM Control Code (DCC)</th>
<th>MSB conversion</th>
<th>MSB-1 conversion</th>
<th>LSB conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>0XX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1XX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>01X</td>
<td>10X</td>
<td>110</td>
<td>111</td>
</tr>
<tr>
<td>11X</td>
<td>101</td>
<td>100</td>
<td>101</td>
</tr>
<tr>
<td>10X</td>
<td>111</td>
<td>110</td>
<td>100</td>
</tr>
</tbody>
</table>
Effect of proposed B-DEM

OSR=16, Mismatch 0.1%
20 times Monte Carlo Simulation

<table>
<thead>
<tr>
<th></th>
<th>SFDR (dB)</th>
<th>SNDR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disable</td>
<td>88.2</td>
<td>83.0</td>
</tr>
<tr>
<td>Enable</td>
<td>103.2</td>
<td>88.5</td>
</tr>
<tr>
<td>Improvement</td>
<td>+15.0</td>
<td>+5.5</td>
</tr>
</tbody>
</table>
Chip photo

- 65nm 9M1P CMOS technology
- Chip area of 0.08mm$^2$
FFT Spectrum

Fs=10MS/s, BW=250kHz, OSR=20, 10kHz input

- SNR=84.2 dB
- SFDR=96.5 dB
- SNDR=83.4 dB

BW=250kHz

Normalized Power [dB]

Frequency [kHz]

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Dynamic range

Dynamic range = 84.2 dB

SNR, SNDR [dB]

Input power [dBFS]
(Fs=10MS/s, OSR=20)
Clock scalability

FoMs > 170 dB for different sampling rates of 2.5 - 25 MS/s.

P_c @ 10MS/s
Analog : 60.0μW (23.3%)
Ref : 35.1μW (13.6%)
Digital : 162.7μW (63.1%)
### Performance Summary

**Recent noise shaping SAR ADC**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Architecture</strong></td>
<td>NS SAR</td>
<td>NS SAR</td>
<td>NS SAR</td>
<td>NS SAR</td>
</tr>
<tr>
<td><strong>Process [nm]</strong></td>
<td>65</td>
<td>28</td>
<td>55</td>
<td>65</td>
</tr>
<tr>
<td><strong>Active Area [mm²]</strong></td>
<td>0.08</td>
<td>0.116</td>
<td>0.072</td>
<td>0.18</td>
</tr>
<tr>
<td><strong>Supply [V]</strong></td>
<td>1.0</td>
<td>1.55/0.75</td>
<td>1.8/1.1</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.8</td>
</tr>
<tr>
<td><strong>Sampling rate [MS/s]</strong></td>
<td>2.5</td>
<td>10</td>
<td>25</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.128</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>BW [kHz]</strong></td>
<td>62.5</td>
<td>250</td>
<td>625</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20</td>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td><strong>SFDR [dB]</strong></td>
<td>88.3</td>
<td>96.5</td>
<td>89.9</td>
<td>111.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>108.0</td>
<td>105.1</td>
<td>86.9</td>
</tr>
<tr>
<td><strong>SNR [dB]</strong></td>
<td>84.3</td>
<td>84.2</td>
<td>82.2</td>
<td>98.57</td>
</tr>
<tr>
<td></td>
<td></td>
<td>94.44</td>
<td>96.8</td>
<td>-</td>
</tr>
<tr>
<td><strong>SNDR [dB]</strong></td>
<td>82.3</td>
<td>83.4</td>
<td>80.4</td>
<td>97.99</td>
</tr>
<tr>
<td></td>
<td></td>
<td>93.95</td>
<td>96.1</td>
<td>76.1</td>
</tr>
<tr>
<td><strong>Power [µW]</strong></td>
<td>66.3</td>
<td>257.8</td>
<td>630.2</td>
<td>37.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>493.1</td>
<td>15.7</td>
<td>1.37</td>
</tr>
<tr>
<td><strong>FoM [dB]</strong></td>
<td>172.0</td>
<td>173.3</td>
<td>170.4</td>
<td>175.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>170.0</td>
<td>180.0</td>
<td>176.8</td>
</tr>
</tbody>
</table>

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Performance comparison

Compared with the state-of-the-art ADCs over 80 dB SNDR

Schreier FoM [dB]

Walden FoM [fJ/conv.]
SAR+$\Delta\Sigma$ ADC for CMOS image sensor

We have applied our proposed ADC technique to CMOS image sensor for reducing the read noise and power reduction.

Proposed ADC for CIS

Low power SAR ADC + low noise $\Delta \Sigma$ ADC

2nd order incremental SAR+$\Delta \Sigma$ ADC
After the SAR conversion, $\Delta \Sigma$ ADC is performed. The signal is sampled and the residue voltage is generated in CDAC using the converted data.
\( \Delta \Sigma \text{ADC} \) is performed in small \( V_q \) of 30 mV with overlapping. The effect of capacitor mismatch is avoided in CDS operation by fixing the CDAC condition for the small signal.

Correlated Double Sampling (CDS)
The ADC is designed in 65 nm CMOS technology.
Measured noise is quite larger than that of the simulated. Our previous SAR+ΔΣADC realized much lower noise.

What is the difference?

<table>
<thead>
<tr>
<th></th>
<th>General purpose [2]</th>
<th>This work for CIS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal: Sampling</td>
<td>Full differential</td>
<td>Single ended</td>
</tr>
<tr>
<td>Signal: Integrator</td>
<td>Full differential</td>
<td>Full differential</td>
</tr>
<tr>
<td>Capacitance (pF): Sampling</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>Capacitance (pF): Integrator</td>
<td>5</td>
<td>0.5</td>
</tr>
<tr>
<td>Signal swing</td>
<td>2 Vpp</td>
<td>1 V</td>
</tr>
<tr>
<td>Quantization voltage (mV)</td>
<td>16</td>
<td>32</td>
</tr>
<tr>
<td>Order of integrator</td>
<td>3</td>
<td>2 (Incremental)</td>
</tr>
</tbody>
</table>
Conclusion

- **Open-loop integrator**
  - 😄 A low gain open-loop amplifier can be used.
  - 😊 No static current, clock scalable by using dynamic amplifiers.
  - 😊 50~90% power reduction compared with conventional closed-loop integrator.

- **Binary-mode DEM**
  - 😄 Simple shuffler
  - 😊 +15dB of SFDR @ OSR=16

- An 84 dB dynamic range, 62.5-625 kHz bandwidth, FoMs > 170 dB noise shaping SAR ADC is realized.

- **SAR+ΔΣADC** is developed for low noise, low power, and high speed ADC for CMOS image sensor.