A stability-improved single-opamp third-order ΣΔ modulator by using a fully-passive noise-shaping SAR ADC and passive adder

Zhijie Chen, Masaya Miyahara, and Akira Matsuzawa

Tokyo Institute of Technology, Japan
Outline

• Motivation
• Traditional implementation
• Proposed architecture
• Circuit and Measurement Results
• Conclusion
Outline

• Motivation
• Traditional implementation
• Proposed architecture
• Circuit and Measurement Results
• Conclusion
Motivation

A sigma delta modulator (SDM) architecture:

- Noise shaping for achieving high resolution
- Usually, 1 opamp --- 1 integrator
- Most of power comes from opamp
- Target: how to reduce power? Reduce No. of opamp?
Outline

• Motivation
• Traditional implementation
• Proposed architecture
• Circuit and Measurement Results
• Conclusion
Single-opamp third-order

A. Pena-Perez, et al., JSSC 2012
Opamp sharing and error feedback

- DAC1
- DAC2
- DAC3
- First Integrator
- Second Integrator
- Feed-forward
- Analog:
  - $1 - Z^{-1}$
  - $Z^{-1}$

- Complex clock gen.
- RDAC, extra power
Stability during non-overlapped time

Opamp : Open-loop state

ста Unstable issue

3rd order, stability?
Outline

• Motivation
• Traditional implementation
• Proposed architecture
• Circuit and Measurement Results
• Conclusion
Architecture

Feed-forward architecture

- 5-bit FPNS SAR ADC, embedded with 1st order NS
- A single opamp is shared to realize 2nd order NS
- A Passive adder to realize FF addition

\[
\int = \frac{0.8z^{-1}}{1-z^{-1}} \quad \int = \frac{2z^{-1}}{1-z^{-1}} \quad \text{NTF}(z) = \frac{1 - 0.5z^{-1}}{1 + 0.5z^{-1}}
\]

\( \oplus \): passive addition
1\textsuperscript{st} order FPNS SAR ADC

Fully passive noise shaping (FPNS) SAR

\[
\text{NTF}(z) = \frac{1 - 0.5z^{-1}}{1 + 0.5z^{-1}}
\]

Z. Chen, et al., VLSIC 2015
A single-opamp 2\textsuperscript{nd} order NS

An opamp sharing technique:

\begin{itemize}
  \item \textbf{A single opamp}
  \item \textbf{1\textsuperscript{st} integrator}
  \item \textbf{2\textsuperscript{nd} integrator}
  \item \textbf{Y}
  \item \textbf{X}
  \item \textbf{C}_4 \& \textbf{C}_5: 1\textsuperscript{st} integrator
  \item \textbf{C}_7 \& \textbf{C}_8: 2\textsuperscript{nd} integrator
  \item \textbf{C}_6: Feed-forward
  \item \textbf{:Additional SC:}
  \item Solve stability issue
  \item \textbf{First Integrator}
  \item \textbf{Second Integrator}
  \item \textbf{Feed-forward}
  \item \textbf{Additional SC}
  \item Non-overlapped
\end{itemize}
A passive adder

A passive adder by capacitor:

\[ X \]

\[ V_{OP} \]

Differential signal:
Input: \( X_P \) & \( X_N \);
Opamp output: \( V_{OP,P} \) & \( V_{OP,N} \);

\[ X_P + V_{OP,P} \]
\[ X_N + V_{OP,N} \]

\[ V_{OP,P} \]
\[ V_{OP,N} \]

\[ V_{OP,P} + X_P = V_{OP,P} - X_N \]
\[ V_{OP,N} + X_N = V_{OP,N} - X_P \]

😊 Passive, save power

Z. Chen, et al., A-SSCC 2012
Outline

• Motivation
• Traditional implementation
• Proposed architecture
• Circuit and Measurement Results
• Conclusion
The schematic

\[ Y(z) = X(z) + \frac{(1 - 0.5z^{-1})(1-z^{-1})^2}{(1+0.5z^{-1})(1+0.6z^{-2})} \]

😊 No RDAC, save power
😊 Only two non-overlapped clocks
😊 No stability issue
The opamp

Current mirror opamp:

Gain = $g_m R_{out} \frac{B}{1 - \alpha}$

$GBW = \frac{g_m}{2\pi C_L} \frac{B}{1 - \alpha}$

$B = \left(\frac{W}{L}\right)_4 \left(\frac{W}{L}\right)_3$

$\alpha = \left(\frac{W}{L}\right)_2 \left(\frac{W}{L}\right)_3$

Single stage, save power

[J. Roh, et al., JSSC 2008]
Chip photo

- CMOS 65 nm, core area: 0.097 mm$^2$

1: 1$^{st}$ sample cap
2: 2$^{nd}$ sample cap
3: Feed-forward cap
4: 1$^{st}$ int. cap
5: 2$^{nd}$ int. cap
6: additional SC

Dimensions:
- Width: 336.6 µm
- Height: 287.9 µm
The measured PSD

Analog power supply: 0.7 V; Digital power supply: 0.85 V

Power Spectral Density

SNDR = 74.94 dB
ENOB = 12.16 bits
OSR = 16
Fs = 3.2 MHz
Fin = 9.95 kHz
BW = 100 kHz

60 dB/Dec

Input signal @ 10kHz
Full scale = 1 V

DR = 78 dB

Peak SNDR: 74.9 dB;

DR: 78 dB

Analog power supply: 0.7 V; Digital power supply: 0.85 V
## Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>[4]</th>
<th>[5]</th>
<th>[1]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (nm)</td>
<td>40</td>
<td>130</td>
<td>180</td>
<td>65</td>
</tr>
<tr>
<td>NS order</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>No. of opamp</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>BW (kHz)</td>
<td>75e3</td>
<td>10e3</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>64.9</td>
<td>75.3</td>
<td>84</td>
<td>74.9</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>22.85</td>
<td>7.19</td>
<td>0.14</td>
<td>0.0458</td>
</tr>
<tr>
<td>Core area (mm²)</td>
<td>0.09</td>
<td>0.08</td>
<td>0.49</td>
<td>0.097</td>
</tr>
<tr>
<td>FoM^W (fJ/conv.-step)</td>
<td>106</td>
<td>75.9</td>
<td>54</td>
<td>50</td>
</tr>
<tr>
<td>FoM^S (dB)</td>
<td>160.1</td>
<td>166.7</td>
<td>172.5</td>
<td>168.3</td>
</tr>
</tbody>
</table>

The fewer No. of opamp is, the lower power is.

Outline

• Motivation
• Traditional implementation
• Proposed architecture
• Circuit and Measurement Results
• Conclusion
Conclusion

- A single-opamp third-order SDM is introduced
  - 74.9 dB SNDR, 3.2-MHz Fs, 50 fJ/Con.-step FoM$^W$, 168 dB FoM$^S$
  - An opamp is sharing to realize 2$^{nd}$ order noise shaping
  - Stability is improved
  - Power efficiency is enhanced
Acknowledgement

This work was partially supported by MIC, HUAWEI, Mentor Graphics for the use of the Analog FastSPICE(AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc, Synopsys, Inc.
Thank you for your interest!

Zhijie Chen,
chen@ssc.pe.titech.ac.jp