Automated Design Strategy for High Performance Mixed Signal Circuits

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Contents

• Background and basic strategy for automated design of mixed signal IPs

• Scalable 12bit SAR ADC for versatile uses

• Layout-driven circuit design and automated layout with regularity

• Fully synthesizable PLL IPs like digital logic gates

• Summary
Background and basic strategy for automated design of mixed signal IPs
Analog front-end can be composed with a few types of mixed signal circuits; only ADC, DAC, PLL, Amplifiers (VGA, Filter).

1) Sensor systems

Sensor → VGA → Filter → ADC

Chopper (option)

M/S: Mixed Signal

2) Receiver

Antenna → LNA → VGA → Filter → ADC

Mixer

Amp.

ADC

DAC

PLL

3) Transmitter

Antenna → VGA → Filter → DAC

Mixer

PLL

Amp.

ADC

DAC

PLL
Background and Motivation

• Issues

It becomes more difficult to obtain good M/S IPs
  – Insufficient design resources (Designers, Tools)
  – Insufficient performance
  – Expensive
  – Longer development time

• Proposed solutions

  – Reduce # of M/S IPs → A few IPs for versatile uses
  – Scalable IPs: performance, power, design rule
  – Reduce the parasitic effect due to layout
  – Automated layout with regularity centric
  – Fully synthesizable IPs like digital logic gates

M/S: Mixed Signal
Selection of the circuits

Select the circuits for high performance automated design

• Low voltage operation
  – Addressable with technology scaling

• Small occupied area
  – Reducible with technology scaling

• Low power
  – Scalable with performance

• Regularity in layout pattern

• Error can be compensated with digital method
Scalable 12bit SAR ADC

for versatile uses
Scalable ADC

Many ADCs to cover the almost all wireless communications.

SNR should be increased by the reduction of BW
P_d should be minimized and reduced by the reduction of BW.

\[ SNR \approx SNR_0 - 10 \log(BW) \]

\[ P_d \approx K_1 \cdot BW \]

\[ K_1: 0.2 \text{ -- } 3 \text{ (mW/MHz)} \]

SAR ADC : ADC for versatile use

SAR ADC is the most energy efficient ADC. It can be used for versatile applications. Conversion errors can be suppressed digitally.

Mismatch CAL. Parasitic CAL. 12bit, 65nmCMOS, 0.03mm²

S. Lee, A. Matsuzawa, SSDM 2013

Logic Comp. CDAC

420μm

70μm

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Use of MOM capacitor

MOM capacitor uses the capacitance between the lateral interconnection. The capacitor density can be increased by technology scaling. Smaller occupied area (same C) can be expected by technology scaling. Furthermore, parasitic capacitance can be controlled.
Dynamic comparator doesn't consume any static power. Large noise was an issue, however can be improved by our proposed circuit using CMOS inter-stage amplifier.


Intermitted operation by self-clocking

Successive comparison is started after the sampling period and ended at 12 conversions. P_d is proportional to the sampling frequency. The leakage current can be blocked by using power gating.

\[ P_d = f_s \times E_d \]

Conversion period

Sampling 2ns

Conversion

12ns: 1.2V

18ns: 1.0V

Power on

End flag

Power off
Scalable power dissipation

$P_d$ is completely proportional to the sampling frequency. Therefore an ultra-low power is possible at low speed operation. Further low power is possible by using low voltage operation.

Suitable for the versatile uses; wireless and sensor

![Graph showing power dissipation vs. sampling frequency](image)

50MSps: 2mW
5MSps: 200uW
500KSp: 20uW
50KSp: 2uW
5kSp: 0.2uW

S. Lee, A. Matsuzawa, et al., SSDM 2013
Performance comparison

- Highest conversion rate: 70MSps
- Lowest voltage: 0.8V
- Lowest $P_d$: 2.2mW at 50MSps
- Smallest FoM: 28fJ
- Smallest area: 0.03mm$^2$

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<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[3]</th>
<th>[4]</th>
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<tbody>
<tr>
<td>Resolution (bit)</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
<td>0.8</td>
<td>1.2</td>
<td>1.2</td>
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<tr>
<td>$f_{sample}$ (MHz)</td>
<td>30</td>
<td>70</td>
<td>45</td>
</tr>
<tr>
<td>$P_d$ (mW)</td>
<td>0.8</td>
<td>2.2</td>
<td>4.6</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>62</td>
<td>65</td>
<td>67</td>
</tr>
<tr>
<td>FoM (fJ) Nyq/DC</td>
<td>81/28</td>
<td>62/33</td>
<td>100/45</td>
</tr>
<tr>
<td>Technology (nm)</td>
<td>65</td>
<td>130</td>
<td>90</td>
</tr>
<tr>
<td>Occupied area (mm$^2$)</td>
<td>0.03</td>
<td>0.06</td>
<td>0.1</td>
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SNR can be increased up to 78 dB by reducing BW. Smallest $P_d$ among ADCs for wireless communications.

84 dB will be attained by dither and DEM method. SNR$_0$ is 140 dB and it can be increased.
Layout-driven circuit design
and automated layout with regularity
Place the components
Route wires between them

1. C1 = 20fF, C2 = 40fF, C3 = 80fF, C4 = 160fF, ...
2. S1 NMOS W/L = 2um/Lmin, S2 = x2, S3 = x4, S4 = x8, ...
3. S1 PMOS W/L = 2um/Lmin, S2 = x2, S3 = x4, S4 = x8, ...
4. Separate each capacitors or shield.
5. Separate between capacitors and digital block or shield.
Issue of conventional idea for analog design

A conventional idea of **Place** the components and **Route** them causes parasitic components essentially and it results in performance degradation.

Parasitic capacitance (3.5 fF)
Between top plate and bottom plates
Causes large conversion error of 50 LSB (12 bit).
Layout driven design with regularity

Avoid wires between components
Wire itself is the component
Respect the regularity and
Pitch should be aligned

Furthermore, if layout has a regularity,
Layout programming becomes easier
Ideal layout design

Pitch is aligned.
It minimizes parasitic component, wire length, delay and capacitance. Low power, high speed, small area, and high robustness can be realized.
Synthesized layout

We can synthesize analog layout by programming

RDAC circuit

Automated optimization
Automated layout with SKILL language

RDAC layout composed by the programming in skill language

Analog circuits

Digital circuits
Automated design for circuit and layout

- Specification
- Process info (PDK)
- Optimization of parameters
- Add digital CAL and TEST circuits

Automated layout programmed in Skill language

- CKT Schematics
- GDS
- Symbol
Circuit schematic and layout

Logic gates should have regularity and launch the automated layout.
Align the layout pitch

Logic gates, DFFs, switches, and resistors are aligned
12 bit R-DAC with automated design

Small 12b R-DAC can be composed by programming in Skill

Simulated DNL and INL (a) without LPE, and (b) with LPE.
LC VCO with MOM capacitor bank

18bit LC VCO without varactors has been developed with MOM capacitors using by programmed layout method.

-1/g_m  L  C_u  2C_u  2^8C_u

Coarse bank

D_c[0]  D_c[1]  D_c[8]

Fine bank

D_r[0]  D_r[1]  D_r[8]

C_s

10kΩ

f_q=6.7kHz@3.3GHz

18bit LC VCO

-121 dBc at 1MHz

Phase noise

MOM capacitance

18bit LC VCO without varactors has been developed with MOM capacitors using by programmed layout method.

Z. Xu, A. Matsuzawa, SSDM 2014.

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Fully synthesizable PLL IPs
like digital logic gates
Small, low jitter, and low power PLL for SoC by using inject locking.

Tj=1.8ps, 1.0 mW, 0.02mm$^2$

Automated circuit and layout design is possible.

W. Deng, K. Okada, A. Matsuzawa, ISSCC 2013

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<td>IL-PLL</td>
<td>DMDLL</td>
<td>DPLL</td>
<td>MDLL</td>
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<tr>
<td>Freq. [GHz]</td>
<td>1.2</td>
<td>1.5</td>
<td>1.5</td>
<td>1.6</td>
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<td></td>
<td>(0.5-1.6)</td>
<td>(0.8-1.8)</td>
<td>(0.8-1.8)</td>
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<td>Ref. [MHz]</td>
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<td>375</td>
<td>375</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>(40-300)</td>
<td></td>
<td></td>
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<tr>
<td>Power [mW]</td>
<td>0.97</td>
<td>0.89</td>
<td>1.35</td>
<td>12</td>
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<tr>
<td>Area [mm$^2$]</td>
<td>0.022</td>
<td>0.25</td>
<td>0.25</td>
<td>0.058</td>
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<tr>
<td>Integ. Jitter [ps]</td>
<td>0.7</td>
<td>0.4</td>
<td>3.2</td>
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<tr>
<td>Jitter RMS/PP [ps]</td>
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<td>0.92/9.2</td>
<td>4.2/33</td>
<td>0.93/11.1</td>
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<tr>
<td></td>
<td>10M hits</td>
<td>5M hits</td>
<td>5M hits</td>
<td>30M hits</td>
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<tr>
<td>FOM [dB]</td>
<td>-243</td>
<td>-248.46</td>
<td>-228.59</td>
<td>-233.76</td>
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<tr>
<td>CMOS Tech.</td>
<td>65nm</td>
<td>130nm</td>
<td>130nm</td>
<td>130nm</td>
</tr>
</tbody>
</table>

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Injection-locked Ring Oscillator

Differential ring VCO with injection locking

W. Deng. ISSCC 2013
Effect of the injection locking

Phase noise is reduced so much by the injection locking

Ref.: 300MHz (40MHz-300MHz) Freq.: 1.2GHz (0.5-1.6GHz)
Integrated jitter: 0.7ps (10kHz-40MHz) Pdc: 0.97mW (1.2GHz)

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Automated design is possible like digital circuits with HDL.

Automated design is possible like digital circuits with HDL.

Verilog netlist (gate-level)

Logic Synt. Tool

Verilog RTL

Logic

Netlist

DCO

Logic

DAC

P&R Tool

GDSII
Low jitter, low power, and small area PLL can be realized with full automated design.

**Integrating Jitter**: 1.7ps
**$P_{DC}$**: 780μW
**FOM**: -236.5 dB

- 110 μm

**Integrating Jitter**: 2.32ps
**$P_{DC}$**: 640μW
**FOM**: -234.6 dB

- 130 μm

Fully synthesized

Hierarchical P&R with synthesized DCOs


W. Deng, K. Okada, A. Matsuzawa, ISSCC 2013
Low FoM and Small area Synthesizable PLL has been developed.
Proposed M/S IP design and business

Circuits should be synthesized automatically. Users can obtain M/S IPs immediately with less money. No limitation for # of design requests.

Input the specification

Users

On the Web

IP Company

Circuits design Program

Status

RDAC: Completed
CDAC: Completed
SAR ADC: Almost completed
OP Amp・Filter: will be developed
PLL: under developing

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Summary

• Issues
   It becomes more difficult to obtain good mixed signal IPs

• Proposed solutions
  – A few mixed signal IPs for versatile uses
    Ex: Scalable 12b SAR ADC for versatile use
  – Regularity driven analog layout
    • Avoid wires between components by using wires as a component
    • Respect the regularity and pitch should be aligned
  – Developed the synthesizable mixed signal IPs programmed in Skill language
  – Developed synthesizable full automated PLL using injection locking, like digital logic design
  – It may create a new IP business model?
Backup slides
Coarse tuning is made by current control
Proposed I-linear DAC

- A **feedback** for forming a **current mirror**.
Tuning Capacitors

Medium resolution

Fine resolution

DM=1

DF=0

DF=1

Vin

VDD

Vin

VDD

(Proposed)

DM=0

4.8ps

V_{in}[V]

0.4ps

V_{in}[V]

0.066ps \times 6

0

10

20

30

Time[ps]

0

10

20

30

Time[ps]
High precision Time to Digital Converter

Charge pump + SAR ADC realizes sub-ps (0.8 ps) TDC
Resolution of conventional inverter based TDC is 10 ps at most.

0.8ps, 10bit, 100Mps, 4mW, 0.02mm²

Low phase noise fractional PLL
On-chip jitter measurement
Sub-mm laser radar

Z. Xu, A. Matsuzawa, CICC 2013.

Nov. 6, 2015.

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