Substrate Noise Isolation Improvement by Helium-3 Ion Irradiation Technique in a Triple-well CMOS Process

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Outline

• Background

• Methods to improve isolation

• Helium-3 ion irradiation

• Simulation results

• Experimental results

• Conclusion
Background

- Analog and digital circuits are integrated on the same chip.
- Increase of digital circuit speed causes more substrate noise coupling problems.
- Analog circuit supply voltage decreases.
Methods to Improve Isolation

• Decreasing noise injection and noise reception
  - Guard rings

• Cutting the propagation path
  - Silicon on insulator (SOI)
    - High cost
  - Proton bombardment
    - High cost
  - Helium-3 ion irradiation
• Cutting the propagation path by increasing the substrate resistivity
• Can be integrated into the standard process
• The design margin is about 15-μm for active device [1].

Helium-3
• high irradiation efficiency
• small dose
• low process cost

Helium-3 Ion Beam from a cyclotron
Helium-3 bombardment from front side to create a high resistive region

Helium-3 Ion Irradiation Machine

Configuration of Irradiation System

(a), (b): Vertical/horizontal scanning magnets
(c), (d), (e): Turbomolecular pumps
(f): Beam shutter
(g), (h): wafer gate valves
(i): Wafer
(j): Automatic wafer handling device

Ref: https://www.shiei.co.jp/english/cyclotron_iis.html
Helium-3 Ion Irradiation Applications

- For inductor
  - Improving inductor quality factor
- For voltage controlled oscillator
  - 8.5dB improvement in phase noise

Substrate Resistivity

- Resistivity after helium-3 ion irradiation

![Graph showing resistivity vs. depth with and without irradiation]

- Dose: $2 \times 10^{13} \text{cm}^{-2}$

- Non-irradiation
- w/ irradiation

- Resistivity after helium-3 ion irradiation
Substrate Resistivity Cont’d

- Resistivity after annealing at 200ºC and 400ºC for 1h.

Graph showing resistivity after annealing at different temperatures and dose. The x-axis represents depth (μm), and the y-axis represents resistivity (Ω·cm). The graph includes lines for non-annealing, annealing at 200ºC for 1h, 400ºC for 1h, and non-irradiation. The dose is 2x10^{13} cm^{-2}.
Isolation Test

(a) diffusion taps

(b) diffusion tap with guard ring at one side

(c) diffusion tap with deep n-well (DNW) guard ring (GR) at one side
EM Simulation

- EM simulator
  - HFSS
- Two-port
- P-diff. taps
  - Area: 35x70μm²
  - Distance: 100μm
- High resistive region
  - Width: 50μm
  - Thickness
    - 65μm
    - 130μm
Simulation Results

- A 10-dB improvement at 2GHz
- As frequency increases, the improvement decreases due to the capacitive coupling
Test Patterns

Top view of test structures

- $W$: diffusion width
- $L$: diffusion length
- $D$: diffusion taps distance

DNW: deep n-well

<table>
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<th>Diff.</th>
<th>Guard Ring (GR)</th>
<th>Dist. ($\mu$m)</th>
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Chip Photo

- A 180-nm standard CMOS process
- Substrate resistivity about 3~4 $\Omega \cdot \text{cm}$
Measurement Results (1)

- Measured noise isolation with respect to tap distance
- Increasing $D$ from 100μm to 150μm improves noise isolation 5dB, from 150μm to 200μm of 3dB at 10GHz
- Increasing $D$ will increase chip area.
Measurement Results (2)

- Measured noise isolation with respect to tap size.
- Large diffusion area causes more coupling.

![Graph](image)

- $S_{21}$ (dB) vs. Frequency (GHz) for different tap sizes:
  - $W=35, L=140$
  - $W=35, L=70$
  - $W=35, L=35$

![Diagram](image)

- Top Metal
- $^3$He$^{2+}$ irrad. region
- Width $W$
- Length $L$
- Distance $D$
Measurement Results (3)

- Isolation is maintained after annealing at 200°C for 1 hour.
Measurement Results (4)

- Isolation is improved for all test patterns after helium-3 ion irradiation.
- A 10-dB improvement (90% noise reduction) is achieved for patterns with GR.
Conclusions

• Helium-3 bombardment is proposed to create a local semi-insulated substrate of high resistibility.

• Noise isolation is improved about 10dB at 2GHz after helium-3 ion irradiation.

• A 90% noise reduction has been achieved for test structures with guard rings.

• The noise isolation can be kept even after annealing at 200°C for 1 hour.
Acknowledgements

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Thank you for your attention