A 9.35-ENOB, 14.8 fJ/conv.-step Fully-Passive Noise-Shaping SAR ADC

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Outline

• Background and motivation
• Conventional Noise shaping technique
• Proposed fully passive noise shaping SAR ADC
• Experimental results
• Conclusion
Background and Motivation

SAR ADC architecture:

- SAR ADC mainly consists of digital circuits
- It can benefit from the technology scaling (like speed)
- Analog components affect the performance
Switch and Capacitor in SAR ADC

Capacitor array affects SAR ADC performance

Switch and Capacitor

- Higher resolution $\rightarrow$ Larger cap $\rightarrow$ Larger settling time
- Larger cap $\rightarrow$ Larger chip size $\rightarrow$ Slower speed
Non-ideal effects further degrade performance.

How to improve the resolution?
Noise shaping technique

Move noise out of band of interest

- Sacrifice speed for resolution
- Noise shaping is based on integrator, usually opamp
Simulation results of non-ideal effects

- Noise shaping reduces non-ideal effects

Comparator noise: $V_n (\sigma(\text{LSB}))$

Settling error (LSB)

DAC mismatch (LSB)

Jitter (ps)

$\text{Fin} = 6.24\text{ MHz}$
Noise shaping effect on capacitance

- Traditional SAR ADC
  \[\text{Thermal noise} = \frac{kT}{C}\]

- Noise shaping SAR ADC
  \[\text{Thermal noise} = (1-Z^{-1}) \frac{kT}{C/OSR}\]

Same SNR, **smaller** capacitor for noise shaping SAR ADC
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Conventional noise shaping technique

- FIR filter introduces extra noise and extra area;
- Opamp: extra power and flicker noise;
- Tech. scaling, difficult to design high performance Opamp

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Traditional architecture

Traditional 1st-order noise shaping architecture

\[ Y = X + (1 - Z^{-1})E \]

\[ Y(N) = X(N) + X_{\text{SAR,in}}(N-1) - Y(N-1) + E(N) \]
Proposed FPNS-SAR ADC architecture

Proposed noise shaping architecture (FPNS-SAR)

⊕ : Realized by Charge redistribution

\[ X_{\text{in}} \]

\[ X_{\text{SAR,in}} = X_{\text{in}} - Z^{-1}E \]

Step 1: Get previous residue on top-plate of C-DAC;
Step 2: Feed it back to input.
Residue in SAR ADC

Residue on the top-plate of SAR ADC

After conversion @ N-1, residue \( V_{top}(N-1) = X_{SAR,in}(N-1) - Y(N-1) \)
FPNS-SAR ADC implementation

1. Conversion @ N-1

After conversion, \( V_{\text{top}} = -E(n-1)/2; \)

2. Clear Charge@ \( \Phi_{\text{NS2}} \)

Clear Charge of \( C_3, Q_{C3} = 0; \)
3. Charge share @ $\Phi_{NS3}$

Get half top voltage, $V_{C3} = V_{top} \cdot (n-1)/2$;

4. Sample @ N

Sampling input, $V_{in}(n)$;
5. Conversion@ N

With the help of \( C_2 \) and \( C_3 \):

\[
V_{DAC}(n) = V_{in}(n) - E(n-1) + E(n)
\]

\[
V_{DAC}(Z) = V_{in}(Z) + (1 - Z^{-1})E(Z)
\]

Realize 1st-order NS
Capacitance comparison

Traditional 10b SAR-ADC

Proposed 10b noise shaping architecture (FPNS-SAR)

\[ C = 8b \text{ C-DAC} \]

\[ C_1 = C_2 = C_3 \]

\[ C_1 < C, \text{ hence, proposal saves area} \]
Circuit details

Total Circuit of FPNS-SAR ADC:

Asynchronous logic; 8-bit C-DAC
Different switches; four inputs comparator
Circuit details

Dynamic comparator [4]

Dynamic comparator, save power

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Chip photograph

230.1 µm

53.4 µm

CMOS 65 nm

CLK

LOGIC

COMP

C-DAC
Experimental results

- Realized 1st-order Noise Shaping

Power Spectral Density

SNDR = 58.03 dB
ENOB = 9.35 bits
Fin = 999.5 kHz
OSR = 4
Fs = 50 MHz
BW = 6.25 MHz

Power supply: 0.8-V
Power: 120.7-µW
## Experimental results - Comparison

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Architecture</td>
<td>SAR</td>
<td>CT-SDM</td>
<td>NS-SAR</td>
<td>FPNS-SAR</td>
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<tr>
<td>Noise Shaping / OTA</td>
<td>No/No</td>
<td>Yes/Yes</td>
<td>Yes/Yes</td>
<td>Yes/ No</td>
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<tr>
<td>Technology (nm)</td>
<td>65</td>
<td>130</td>
<td>65</td>
<td>65</td>
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<tr>
<td>Bandwidth (MHz)</td>
<td>0.5</td>
<td>15.6</td>
<td>11</td>
<td>6.25</td>
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<tr>
<td>Core Area (mm²)</td>
<td>0.0259</td>
<td>0.27</td>
<td>0.0323</td>
<td>0.0123</td>
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<tr>
<td>Supply (V)</td>
<td>1</td>
<td>1.3</td>
<td>1.2</td>
<td>0.8</td>
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<tr>
<td>Power (µW)</td>
<td>1.9</td>
<td>4000</td>
<td>806</td>
<td>120.7</td>
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<tr>
<td>ENOB (bits)</td>
<td>8.75</td>
<td>9.6</td>
<td>10</td>
<td>9.35</td>
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<tr>
<td>FoM² (fJ/conv.)</td>
<td>4.42</td>
<td>160</td>
<td>35.8</td>
<td>14.8</td>
</tr>
</tbody>
</table>

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• First work that realizes *Passive* noise shaping SAR, save power;

• Maintain basic architecture and operation of SAR-ADC, inherits advantage of SAR-ADC;

• No Opamp, most are digital circuits, robust to future technology and power supply downscaling;

• Relax the requirement of circuit blocks, save area and save power.
Acknowledgements

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