Delta-Sigma Time to Digital Converter Using Charge Pump and SAR ADC

IEICE General Conference 2015
Anugerah Firdauzi, Zule Xu, Masaya Miyahara, and Akira Matsuzawa
Tokyo Institute of Technology
Outline

• Background
• Basic concept
• Circuit design
• Simulation results
• Conclusion
Background

- **TDC Application**
  - 3D camera
  - Laser range finder
  - Time-of-flight (TOF) particle detector
  - On chip jitter measurement
  - PLL and frequency synthesizer

- **Contradictory requirements**
  - High resolution (~1ps)
  - Wide input range (several ns)
Previous Work

- Charge pump and SAR ADC
- Time-to-charge conversion with SAR ADC → high resolution
- SAR-ADC: compact, sufficient range, and moderate speed
- Challenge: high order SAR ADC is required
  - High design complexity
  - Limited speed
  - Large area

\[ t_{res} = C \cdot V_{LSB} / I \]

[Z.Xu, CICC '13]
Proposal: $\Delta \Sigma$ TDC

- $\Sigma$ is realized by charging capacitor $C$ and never reset it
- $\Delta$ is realized by discharging/charging $C$ through array of current source DAC at constant time for positive/negative output
Timing Diagram

- \[ \Delta V_{\text{max}} = \Delta V_{\text{IN, max}} + \Delta V_{\text{DAC, max}} \]
- \[ \frac{1}{2} (V_{\text{refp}} - V_{\text{refn}}) = \frac{I_{\text{CP}} \cdot T_{\text{IN, max}}}{C_{\text{DAC}}} + \frac{\Sigma I_{\text{DAC}} \cdot T_{\text{DAC}}}{C_{\text{DAC}}} \]

**\( \Delta \Sigma \) thumb rule:**

\[ |\Delta V_{\text{IN, max}}| = |\Delta V_{\text{DAC, max}}| \]

For VOP:
1. Charging input
2. HIGH output \( \rightarrow \) discharge
3. LOW output \( \rightarrow \) charge

4/2/2015

Anugerah Firdauzi - Tokyo Tech
**Multibit Quantizer Effect**

- **For** \( L^{th} \) **order ΔΣ ADC with** \( N \) **bit quantizer:**
  - \( SNR_{dB} = 10 \log \left( \frac{3\pi}{2} (2^N - 1)^2 (2L + 1) \left( \frac{OSR}{\pi} \right)^{2L+1} \right) \)
  - \( ENOB = (SNR_{dB} - 1.76)/6.02 \)
- **Increasing quantizer size by one can improve** \( ENOB \) **1-1.5 bit**

---

**Target:**
- 1\(^{st}\) order ΔΣ TDC
- Quantizer 4 bit
- OSR = 100
- ENOB = 13 bit
Simulation Result

• Ideal model using MATLAB
• 4 bit quantizer
• Input = ±1ns at 52kHz
• BW = 1MHz
• OSR = 100

• Result:
  ➢ ENOB > 11bit
  ➢ Effective resolution < 0.9ps

![Simulation Result Graph]

SNDR = 72.42 dB
ENOB = 11.74 bit
SNDR = 73.63 dB
ENOB = 11.94 bit

1ps noise
ideal
20dB/dec
1ns input
BW

10^4 10^5 10^6 10^7 10^8
Frequency [Hz]
PSD [dB]

SNDR = 72.42 dB
ENOB = 11.74 bit
SNDR = 73.63 dB
ENOB = 11.94 bit
Conclusion

- A new approach for TDC by using $\Delta \Sigma$ architecture is proposed.

- $\Delta \Sigma$ TDC implemented by using CP SAR ADC, and current source DAC gives first order noise shaping and high resolution for moderate bandwidth while keeping the input range large and power consumption low.