A 0.048-mm$^2$ 3-mW Synthesizable Fractional-\(N\) PLL with a Soft Injection-Locking Technique

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Outline

• Introduction
• Concept of Soft Injection Locking
• Circuit Implementations
• Measurement Results
• Conclusion
Introduction

• Why High Performance PLL
  – Clock generation/distribution

• Key Specifications for SoC Clocking
  – Small area
  – Low power consumption
  – Low jitter
  – Insensitive over environment variations
  – Scalable with technology advancement
All-digital PLLs

- TDC-based architecture

- Taking advantages of digital circuits
- Compact chip area
- Cannot fully utilize digital design flow
  - Layout uncertainty caused by Auto Place & Route degrades TDC and DCO linearity.
Injection Locking Technique

Free-running VCO

Injection locked

Offset Frequency

Phase noise

Injection locked

Free-running

$\frac{\sqrt{6/(N(N-1))}}{2\pi} \cdot f_{\text{ref}}$

[N.D. Dalt, TCAS II 2014]
Phase Noise Comparison

Free-running oscillator

Freq_{ref} = 100MHz
Freq_{DCO} = 1GHz
FOM_{DCO} = -153 dB
(-90dBc/Hz at 1MHz, 0.5mW)

Jitter_{TDC-PLL} = 6.4ps
Jitter_{IL-PLL} = 1.5ps
Injection Method

• Pulse Injection [B. Helal, et al., JSSC 2009]

• Multiplying DLL [S. Ye, et al., JSSC 2002]

• Edge Injection [W. Deng, et al., ISSCC 2014]
Integer-\(N\) Operation

e.g. \(N=3\)

Reference

VCO

\[ \text{e.g. } N=3 \]
Sub-Integer-\(N\) Operation

\[
\text{Reference} \xrightarrow{\text{D}} \text{P}_0 \xrightarrow{\text{D}} \text{P}_1 \xrightarrow{\text{D}} \text{P}_2 \xrightarrow{\text{...}} \text{D} \\
\]

\[\text{e.g. } N=3+(1/M)\]

Reference

P_0

VCO

P_1

P_2

\[
\ldots
\]

[P. Park, et al., ISSCC 2012]
Phase Domain (Integer-$N$)

\[ \phi_{PLL} \]

\[ f_{PLL} = N \cdot f_{ref} \]

\[ T_{ref} \]

\[ 2 \cdot T_{ref} \]

\[ 3 \cdot T_{ref} \]

\[ 4 \cdot T_{ref} \]

\[ 5 \cdot T_{ref} \]

P0 → P0 → P0 → P0 → P0 → P0 → P0 → P0 → P0 → P0...

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Phase Domain (Sub-Integer-$N$)

\[ f_{PLL} = \left( \frac{N+1}{M} \right) \cdot f_{ref} \]

P0 $\rightarrow$ P1 $\rightarrow$ P2 $\rightarrow$ P3 $\rightarrow$ ... $\rightarrow$ P0 $\rightarrow$ P1 ...
Phase Domain (Fractional-N)

\[
f_{PLL} = \left( \frac{N+0.5}{M} \right) \cdot f_{ref}
\]

\[
\phi_{PLL} = \left( \frac{4N+2}{M} \right) \cdot 2\pi
\]

\[
\phi_{PLL} = \left( \frac{3N+1}{M} \right) \cdot 2\pi
\]

\[
\phi_{PLL} = \left( \frac{2N+1}{M} \right) \cdot 2\pi
\]

\[
\phi_{PLL} = N \cdot 2\pi
\]

\[
T_{ref} \rightarrow 2 \cdot T_{ref} \rightarrow 3 \cdot T_{ref} \rightarrow 4 \cdot T_{ref} \rightarrow 5 \cdot T_{ref}
\]

P0 → P0 → P1 → P1 → P2 → P2 → P3 ...

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Time Domain (Fractional-$N$)

- Spur is caused by “hard” switching
Proposed Soft Injection

Reference → Soft Injection → Injection Signal

Reference

Soft Injection signal

Locked
"Hard" vs "Soft" Injection

Injection at $\phi_0$  Injection at $\phi_{10}$

Reference

$\phi_{10}$ w/o inj

$\phi_{10}$ w/ inj

Conventional "hard" injection

Soft injection

$\phi_{10}$ w/o inj

$\phi_{10}$ w/ inj

Proposed "soft" injection
Injection Strength

• Soft injection signal level determines injection strength

Soft Injection Signal

• Stronger injection strength leads to larger phase shift
Fractional-$N$ Operation (Hard)

- Selected injection phase
- Available injection phase

\[ f_{PLL} = (N + 1.5/28) \cdot f_{ref} \]

\[ f_{PLL} = (3N + 7/28) \cdot 2\pi \]
\[ f_{PLL} = (3N + 6/28) \cdot 2\pi \]
\[ f_{PLL} = (3N + 5/28) \cdot 2\pi \]
\[ f_{PLL} = (3N + 4.5/28) \cdot 2\pi \]
\[ f_{PLL} = (3N + 3/28) \cdot 2\pi \]
\[ f_{PLL} = (3N + 2/28) \cdot 2\pi \]
A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Fractional-N Operation (Soft)

- Selected injection phase
- Available injection phase

\[ f_{PLL} = \left( N + \frac{1.5}{28} \right) \cdot f_{ref} \]

\[ \phi_{PLL} = \left( 3N + \frac{7}{28} \right) \cdot 2\pi \]
\[ \left( 3N + \frac{6}{28} \right) \cdot 2\pi \]
\[ \left( 3N + \frac{5}{28} \right) \cdot 2\pi \]
\[ \left( 3N + \frac{4.5}{28} \right) \cdot 2\pi \]
\[ \left( 3N + \frac{4}{28} \right) \cdot 2\pi \]
\[ \left( 3N + \frac{3}{28} \right) \cdot 2\pi \]
\[ \left( 3N + \frac{2}{28} \right) \cdot 2\pi \]
PLL with Soft Injection

- Cascading topology

Reference Clock

MDLL

Soft-Injection

Gating

DSM

Frequency-locked Loop

0.8-1.7GHz

328 Phases

100-600MHz

1× ~ 12×
**Effective soft injection signal** is generated by soft injection generator and gating array.

- **Soft Injection Generator**

```
  N1·REF
    |   MUX
    |   MUX
    |   MUX
    |   DQ
    |   Reset
    |   VDD
    |   Gating Array
    |   Injection signal
```

Digital varactor
Fractional-$N$ Controller

- **Dither**
- **DSM**
- **Sub Integer**
- **FCW**
- **Gating Array**
- **Ref**
- **MDLL**
- **Retimer**
- **Deglitching**
- **Mapping**
Gating Array

Soft Injection generator

Frac-N Controller

Interpolative phase coupled DCO

DAC
Interpolative phase coupled DCO

- Standard cell design
- Interpolative phase coupling for accurate phase

[W. Deng, et al., ISSCC 2014]
Design Procedure

Logic

Verilog RTL

Logic Synt. Tool

Verilog netlist (gate-level)

DCO

Logic

Logic Synt. Tool

Verilog netlist (gate-level)

Logic

Netlist

P&R Tool

GDSII

Netlist
Chip Microphotograph

65nm CMOS technology
Phase Noise

Frequency: 1.2576 GHz
Integrated Jitter: 2.5 ps
$P_{DC}: 2.9 \text{ mW}$
Spur against Inj. Strength

![Graph showing spurious output level against injection strength](image)

<table>
<thead>
<tr>
<th>Spur Level [dB]</th>
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</thead>
<tbody>
<tr>
<td>-60</td>
</tr>
<tr>
<td>-50</td>
</tr>
<tr>
<td>-40</td>
</tr>
<tr>
<td>-30</td>
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</table>

<table>
<thead>
<tr>
<th>Inj. Strength Control Code</th>
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<tbody>
<tr>
<td>(Soft)</td>
</tr>
<tr>
<td>(Hard)</td>
</tr>
<tr>
<td>001</td>
</tr>
<tr>
<td>011</td>
</tr>
<tr>
<td>101</td>
</tr>
<tr>
<td>111</td>
</tr>
</tbody>
</table>

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Jitter against Inj. Strength

![Graph showing Jitter against Inj. Strength](image)

- Integrated Jitter [pS]
- Inj. Strength Control Code
- (Soft) 001 011 101 111 (Hard)

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## Comp. of Synthesizable PLLs

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[1]</th>
<th>[2]</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm</td>
<td>65nm</td>
<td>65nm</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>2.9 @1.2576GHz</td>
<td>0.78 @0.9GHz</td>
<td>13.7 @2.5GHz</td>
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<tr>
<td>Area [mm²]</td>
<td>0.048</td>
<td>0.0066</td>
<td>0.04</td>
</tr>
<tr>
<td>Integ. Jitter [ps]</td>
<td>2.5</td>
<td>1.7</td>
<td>3.2*</td>
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<tr>
<td>FOM [dB]</td>
<td>-227</td>
<td>-237</td>
<td>-219*</td>
</tr>
<tr>
<td>Topology</td>
<td>Soft-IL</td>
<td>IL</td>
<td>TDC-based</td>
</tr>
<tr>
<td>Type</td>
<td>Frac-N</td>
<td>Integer-N</td>
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<tr>
<td>Synthesized?</td>
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</table>

*FOM is calculated based on RMS jitter.

Conclusion

• A synthesizable fractional-N PLL with a soft-injection locking technique is presented.

• The soft injection locking technique provides potentials for future clock generation circuit designs.
Acknowledgement

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