An HDL-Synthesized Gated-Edge-Injection PLL with A Current Output DAC

Dongsheng Yang, Wei Deng, Tomohiro Ueno, Teerachot Siriburanon, Satoshi Kondo, Kenichi Okada, and Akira Matsuzawa

Tokyo Institute of Technology, Japan
Conventional All-digital PLLs

• TDC-based architecture

– The layout uncertainty degrades TDC and DCO linearity.

• Trade-off between layout area and jitter performance
Proposed IL-based Synthesizable PLL

Injection-Lock (IL) architecture is employed

Pulse $\rightarrow$ Edge

FLL with Offset Calibration

Cell-based I-DAC

Feedback FLL for frequency tracking
Feedforward edge injection for phase locking

[W. Deng, et al., ISSCC 2014]
A feedback structure for forming a current mirror.

[W. Deng, et al., ISSCC 2014]
## Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power [mW]</strong></td>
<td>0.78 @900MHz</td>
<td>13.7 @2.5GHz</td>
<td>3.1 @250MHz</td>
<td>2.1 @403MHz</td>
</tr>
<tr>
<td><strong>Area [mm²]</strong></td>
<td>0.0066</td>
<td>0.042</td>
<td>0.032</td>
<td>0.1</td>
</tr>
<tr>
<td><strong>FOM [dB]</strong></td>
<td>-236.5</td>
<td>-218.6*</td>
<td>-205.5</td>
<td>-214*</td>
</tr>
<tr>
<td><strong>W/ custom cells?</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Topology</strong></td>
<td>IL-base</td>
<td>TDC-base</td>
<td>TDC-base</td>
<td>TDC-base</td>
</tr>
</tbody>
</table>

*FOM is calculated based on RMS jitter.

The proposed HDL-synthesized PLL can achieve the smallest area with comparable FOM.