Digitally Assisted Wireless
Transceivers and Synthesizers

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Outline

- Analog to Digital
  - Digitization of Wireless TRX
- Digital Assistance
  - Wireless Transceiver
  - Frequency Synthesizer
- Future Analog Design
  - Synthesizable Analog
Analog to Digital

Digitization

- Scalability
- Portability

Digital Assistance

- Robustness
- Less redundancy
Further Digitization

Digitization

- Scalability
- Portability

Massive Digital Assistance

- Robustness
- Less redundancy

Analog

Digital

Digital
Case Study

Partially replaced by pure digital-domain “calculation” (NOT time-domain analog processing)

- Filter: LPF in AD-PLL, LPF in wireless TX
- Equalizer: FIR in wireless, OFDM
- PLL: carrier and timing recovery in wireless RX
- Mixer: Low-IF transceiver

Only analog-domain

- Oscillator: Clock generation
- Data converter: V-to-D, D-to-V, D-to-I, C-to-D, ...
- Analog amplifier: voltage-to-voltage

Difficult for digitization
History of Timing Recovery


Analog recovery

Digitally-assisted analog recovery

Digital recovery

Analogue processing

Digital processing

Sampling clock

Timing recovery

Analog Demodulator

Costas-loop for BPSK


timing recovery loop (carrier & phase)
Digital Carrier and Timing Recovery

Everything is implemented in digital domain.

Timing recovery (phase)  Carrier recovery (freq.)

ADC → interpolation filter → timing-recovered signal → NCO → LF → PD → NCO → rotation filter → timing- & carrier-recovered signal → ADC


NCO: Number-Controlled Oscillator
LF: Loop Filter
PD: Phase Detector
Recent Digital Transceiver

Analog

RX ADC
ADC
TX DAC
DAC
LPF
LPF
VGA
VGA
LPF
LPF
Analog Digital
RX filter
TX filter
Carrier & Timing Recovery
Demapper
FEC Decoder
Mapper
FEC Encoder
Zero-IF
LPF for transmitting bandwidth restriction
Digitization of IF Mixer

Hetero-dyne RX

Low-IF RX

Very common for BT
1/f noise
Overhead for ADC
Aim of This Talk

• **Digitization**
  - Wireless transceiver is a good example of digitized analog circuit. (for hinting)

• **Digital assistance**
  - Digital calibration/compensation is implemented in a system level to satisfy complicated requirements for wireless system.
  - Mutual re-use of TX and RX for calibration

• **Digitally-designed analog**
  - Toward “Synthesizable Analog Circuit”
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Impairments in Wireless Transceiver

Mismatch in differential block
- DC offset in RX
- IIP2 in RX
- LO leakage in TX

Mismatch btw I and Q blocks
- Image signal
- Analog filter BW (LPF)

Non-linearity
- IMD in PA

PVT variation
- Gain control
- Power control
- VCO LC tank
- ILFD/ILO

Environmental variation
- TX-to-RX distance
- Fading
- Antenna reflection

*A. Jerng, “Digital Calibration for RF Transceivers,” ISSCC 2012, Tutorial 9*
Digital Equalizers

Adaptive RF&BB equalizer

Environmental Variation
Fading by multi-path
flat or frequency selective

RF&BB equalizer
Automatic Gain Control (AGC)

Analog
- VGA
- LPF
- ADC
- DAC
- LPF
- VGA
- LPF

Digital
- RX filter

Environmental Variation
- Received signal strength
- Antenna reflection

Automatic Gain Control
DC offset cancel
I/Q Mismatch

Analog

Digital

RX
ADC
ADC
TX
DAC
DAC

Digital BB

phase mismatch

gain & phase mismatch
Image Rejection Ratio (IMRR)

\[ \Delta \text{IMRR} = \Delta \text{LO} - \Delta \text{BB} \] [dBm]

\[ \text{freq. [GHz]} \]

\[ \omega_{LO} - \omega_{BB} \quad \omega_{LO} \quad \omega_{LO} + \omega_{BB} \]

Desired

LO leak

Image

IMRR [dB]

e.g. \( \omega_{BB} = 10\text{MHz} \)
I/Q mismatch degrades SNR.

\[ \Delta \text{LO} - \Delta \text{BB} \quad [\text{dBm}] \]
\[ \text{freq.} \quad [\text{GHz}] \quad \Delta \text{LO} + \Delta \text{BB} \]

**Desired**

**IMRR [dB]**

**Image**
Image Rejection Ratio (IMRR)

\[ |\text{IMRR}| \approx \frac{\Delta g^2 + \Delta \theta^2}{4} \]

\(\Delta g\): Amplitude error ratio
\(\Delta \theta\): Phase error

Target:
0.2dB, 1.0degree
for IMRR of 35dB
TX IMRR Calibration

I: 0°
Q: -90°

Test signal coupler

TX

Down-conversion is required.
Detector can be used.
(2nd-order distortion)

Desired freq. [GHz]

\( \omega_{LO} - \omega_{BB} \)
\( \omega_{LO} + \omega_{BB} \)
\( \omega_{LO} \)

LO
IM

freq. [GHz]
TX IMRR Calibration

I: 0°
Q: -90°

test signal
coupler
Detector

\[
\begin{align*}
\omega_{LO} - \omega_{BB} & \quad \omega_{LO} + \omega_{BB} \\
\omega_{LO} & \quad 0 & \quad \omega_{BB} & \quad 2\omega_{BB}
\end{align*}
\]
Detector

$\nu_{out} = \text{LPF}(A \nu_{in}^2)$

RF (e.g. 5GHz)  
LO  
IM  
Desired

$\omega_{LO} - \omega_{BB}$  
$\omega_{LO} + \omega_{BB}$  
$\omega_{LO}$

LPF  
BB (e.g. 10MHz)

$\nu_{out} = \text{LPF}(A \nu_{in}^2)$

Desired

$\omega_{BB}$  
$2\omega_{BB}$

$v_{out} = \text{LPF}(A v_{in}^2)$
I/Q Mismatch Calibration by Loop-back

- I/Q Amplitude offset
- I/Q Phase offset
I/Q Mismatch Calibration by Loop-back

- I/Q Amplitude offset
- I/Q Phase offset

5% cut-off mismatch causes a serious frequency-dependent I/Q mismatch.
Gain/phase mismatch can be frequency-dependent.

5% cut-off frequency mismatch
-37dB@1MHz, -27dB@10MHz
Key Idea of Wireless Calibration

Self-calibration with less additional blocks
Reuse of TRX each other

TX = Signal Generator for RX calibration
RX = Spectrum Analyzer for TX calibration
1. **RX BB LPF** Calibration (using TX BB)
   - I/Q gain mismatch
   - LPF cut-off mismatch (including VGA and ADC)

2. **TX BB LPF** Calibration (using RX BB)
   - I/Q gain mismatch
   - LPF cut-off mismatch

3. **TX I/Q** Calibration (using detector and RX BB)
   - Impairments of mixer, LO, RF I/Q amps., etc
   - compensated by **digital BB**

4. **RX I/Q** Calibration (using TX)
   - Impairments of mixer, LO, RF I/Q amps., etc
   - compensated by **digital BB**
VGA and ADC are also included in RX BB calibration.
TX Filter Calibration (BB loopback)

LPF gain/cut-off mismatch between I/Q paths are calibrated.
RF Loop-Back Calibration for TX

ADC is re-used for IM/LO calculation with DFT in BB.

Detector

compensate

target

RF Loop-Back Calibration for TX

RF Loop-Back Calibration for RX

TX is used for a test-tone generator.

At least, a **10-bit ADC** is required for a IMRR of 40dB.

**LPF**$\begin{align*}
(I^2 + Q^2)
\end{align*}$

**RSSI** $\rightarrow$ **AGC**

**LPF**$\begin{align*}
(I^2 - Q^2)
\end{align*}$ $\approx \Delta g$

**LPF**$\begin{align*}
(I \ast Q)
\end{align*}$ $\approx -\Delta \theta / 2$

Modulated signal can be used.

$\rightarrow$ **Background calibration**

*S. Lerstaveesin, et al., IEEE JSSC 2006.*
RF Loop-Back Calibration for RX

Calibration vs Compensation

Frequency independent (RF)
TX I/Q mismatch(RF) $\rightarrow$ Digital compensation (BB TX filter)
RX I/Q mismatch(RF) $\rightarrow$ Digital compensation (BB RX filter)
FDE/OFDM

Frequency independent (BB)
TX I/Q mismatch(BB) $\rightarrow$ Digital compensation
RX I/Q mismatch(BB) $\rightarrow$ Digitally-calibrated analog (AGC)
/ Digital compensation

Frequency dependent (BB)
TX I/Q mismatch(BB) $\rightarrow$ Digitally-calibrated analog
RX I/Q mismatch(BB) $\rightarrow$ Digitally-calibrated analog
/ Digital compensation

as a typical case
60GHz Transceiver Calibration

One additional ADC is used for a fine resolution.

*T. Tsukizawa, et al., ISSCC 2013
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  • Synthesizable Analog
Calibration in Frequency Synthesizer

- AFC for capacitor-bank in LC-VCO
- ILFD/ILO Calibration
- Linearity calibration/compensation
  - Loop-BW, Quantization noise, FM/Polar-TX

\text{VCO: frequency} \leftarrow \text{voltage (varactor, C-bank)}
\text{DCO: frequency} \leftarrow \text{code (C-bank, I-control)}
\text{TDC: code} \leftarrow \text{delay (PVT, noise, layout, etc)}
(\text{ADC: code} \leftarrow \text{voltage})
(\text{DAC: voltage} \leftarrow \text{code})
(\text{Amp: voltage} \leftarrow \text{voltage})

AFC: Automatic Frequency Calibration
ILFD: Injection-Locked Frequency Divider
ILO: Injection-Locked Oscillator (Multiplier)
ILFD Calibration

Locked*/Free-run** frequency is used.

60GHz PLL

*S. Pellerano, et al., ISSCC 2008 **T. Shima, et al., APMC 2011
Summary of Transceiver Calibration

• Wireless transceiver is a big system.
• Historically, architecture-level digitization has been applied with system-level calibration and compensation for PVT and environmental variations.
• Re-use of counter-part block for calibration
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Issues of Analog Circuit Design

Why is the simulated performance degraded?

Imperfection caused by physical implementation

PVT

layout non-ideality

• mismatch

• isolation/coupling

Compensated by digital assistance
Transistor matching cannot be expected any more.

- Larger Rd, Rs, Rg
- Fixed fin height (for FinFET)
- Self-heating
- No body effect
Scaled CMOS Layout

65nm layout style

- Uni-directional features
- Uniform gate dimension
- Gridded layout

32nm layout style

*M. Bohr, ISSCC 2009*
Massive Digital Assistance

PVT layout non-ideality
• mismatch
• isolation/coupling

Compensated by digital assistance

Delay and linearity in delay can be calibrated easily in time-domain analog circuits, e.g. AD-PLL.
Further Analog Circuit

Digitization

- Scalability
- Portability

Massive Digital Assistance

- Robustness
- Less redundancy
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Synthesizable Analog Circuits

HDL

module PLL (CLK, ..., OUT)
...
endmodule

Digital design flow

Commercial P&R tools…

GDS

with a standard-cell library
without any custom-designed cells
without manual placement
Analog Synthesis by Digital Tools

Pure digital

Logic

Verilog RTL

Logic Synt. Tool

DCO

Verilog netlist (gate-level)

Digitally-designed Analog

Logic

Netlist

P&R Tool

GDSII

Layout uncertainty

*W. Deng, et al., ISSCC 2014
Massive digital assistance can overcome the layout uncertainty issue. 

- Unbalanced loading
- No layout symmetry

Ideal placement

Actual placement

e.g., DCO & TDC linearity
Synthesizable Analog Circuits

only by standard cells

• Synthesizable PLL*
• Synthesizable DCO
• Synthesizable DAC
• Synthesizable TDC
• Synthesizable ADC**

*W. Deng, et al., ISSCC 2014 **S. Weaver, et al., IEEE TCAS-I 204
Synthesizable ADC

ADC architecture
SNDR of 35.9dB, 210MS/s

Comparator by NAND3
Gaussian offset distribution

Linearity compensation by inverse Gaussian

*S. Weaver, et al., IEEE TCAS-I 2014
Synthesizable DCO

*MUX and varactor*  
Path-Selection MUX

Phase-Interpolator**, I-DAC***, and fine varactor***

*D. Sheng, et al., IEEE TCAS-II 2007
Synthesizable DAC

Only standard cell

\[ \begin{align*}
D_0 &= 0 \quad V_{out} = 1V \\
D_0 &= 1 \quad V_{out} = 0V
\end{align*} \]

\[ \begin{align*}
D_0D_1 &= 11 \quad V_{out} = 0V \\
D_0D_1 &= 10 \quad V_{out} = 0.5V \\
D_0D_1 &= 01 \quad V_{out} = 0.5V \\
D_0D_1 &= 00 \quad V_{out} = 1V
\end{align*} \]
Synthesizable I-linear DAC

Only standard cell

D0 \times 1
D1 \times 2
D2 \times 4
D3 \times 8

V_{out}

Current-starving RO by NAND2

\*W. Deng, et al., ISSCC 2014

I_{out}

*W. Deng, et al., ISSCC 2014
V-linear DAC vs I-linear DAC

Current-starving RO by NAND2
1.55ps@200MHz

*P. L. Chen, et al., TCAS II 2005
Performance Trade-off

- Custom design
- Custom design but easy
- Synthesizable design

Performance A vs. Performance B
A synthesis-friendly architecture can improve performances.
Injection-Locked PLL (IL-PLL)

Conventional CP-PLL and TDC-PLL (AD-PLL)
- Phase lock: feedback
- Frequency lock: feedback

Injection-Locked PLL (IL-PLL)
- Phase lock: feed-forward ← Injection-lock
- Frequency lock: feedback ← Counter

The fine timing feedback is not required.

→ Synthesis-friendly

*W. Deng, et al., ISSCC 2014
Injection-Locked PLL

\[ f_{\text{ref}} \overset{\sim}{\longrightarrow} f_{\text{out}} = N \cdot f_{\text{ref}} \]

**Reference injection**

**Noise folding**

& phase lock

Flicker of \( PN_{\text{VCO}} \) & Ref noise

\[ PN_{\text{ref}} + 20 \log_{10}(N) \]

\[ 0.4 \cdot f_{\text{ref}} \]

Offset Freq. [Hz]

Phase noise [dBc/Hz]

*S. Ye, et al., IEEE JSSC 2002  **N. D. Dalt, IEEE TCAS-II 2014*
Synthesizable IL-PLL

Frequency tracking with very narrow BW

Gated Edge Injection

Severe timing design is NOT required.

CMOS 65nm
Area: 0.0066mm$^2$
Jitter: 1.7ps
$P_{DC}$: 780μW
FOM: -236.5 dB

60μm
110μm
60μm
Comparison of the state-of-the-art PLLs

*W. Deng, et al., ISSCC 2014

Better performance

This work
Synthesized PLL

Synthesized PLL

Synthesized PLL

Synthesized PLL

Synthesized PLL

Synthesized PLL

Synthesized PLL
### Comparison of Synthesizable PLL

<table>
<thead>
<tr>
<th></th>
<th>This work 65nm</th>
<th>[22] 28nm</th>
<th>[23] 65nm</th>
<th>[24] 65nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power [mW]</strong></td>
<td>0.78 @900MHz</td>
<td>13.7 @2.5GHz</td>
<td>3.1 @250MHz</td>
<td>2.1 @403MHz</td>
</tr>
<tr>
<td><strong>Area [mm²]</strong></td>
<td>0.0066</td>
<td>0.042</td>
<td>0.032</td>
<td>0.1</td>
</tr>
<tr>
<td><strong>Integ. Jitter [ps]</strong></td>
<td>1.7</td>
<td>N.A.</td>
<td>30</td>
<td>N.A.</td>
</tr>
<tr>
<td><strong>RMS Jitter [ps]</strong></td>
<td>2.8</td>
<td>3.2</td>
<td>N.A.</td>
<td>13.3</td>
</tr>
<tr>
<td><strong>FOM [dB]</strong></td>
<td>-236.5</td>
<td>-218.6*</td>
<td>-205.5</td>
<td>-214*</td>
</tr>
<tr>
<td><strong>W/ custom cells?</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Topology</strong></td>
<td>IL-base</td>
<td>TDC-base</td>
<td>TDC-base</td>
<td>TDC-base</td>
</tr>
</tbody>
</table>

*FOM is calculated based on RMS jitter.
Conclusion

• Digitization vs Digitally-Assisted Analog
• Digitally-Assisted Analog to Digitally-Designed Analog
e.g. Synthesizable Analog Circuit
  portability, scalability, robustness,..
References


References


References


References


Other example:

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Appendix
Up-conversion by $\cos(\omega_{\text{LO}} t)$

$\quad$

\[ \cos(\omega_{\text{BB}} t) = \frac{e^{i\omega_{\text{BB}} t} + e^{-i\omega_{\text{BB}} t}}{2} \]

\[ \quad \times \cos(\omega_{\text{LO}} t) = \frac{e^{i\omega_{\text{LO}} t} + e^{-i\omega_{\text{LO}} t}}{2} \]

\[ 2e^{-j\omega_{\text{LO}} t} \]

\[ e^{j\omega_{\text{LO}} t} \]

$\quad$

\[ \cos(\omega_{\text{BB}} t) \times \cos(\omega_{\text{LO}} t) \]
Up-conversion by $\sin(\omega_{LO} t)$

\[
\sin(\omega_{BB} t) = \frac{-je^{j\omega_{BB} t} + je^{-j\omega_{BB} t}}{2}
\]

\[
* \sin(\omega_{LO} t) = \frac{-je^{j\omega_{LO} t} + je^{-j\omega_{LO} t}}{2}
\]

\[
\sin(\omega_{BB} t) * \sin(\omega_{LO} t)
\]
Ideal I/Q Up-Conversion

-90°

Image signals are canceled.
Image signals are NOT canceled.
Calibration of Injection Lock Oscillator

*W. Deng, et al., A-SSCC 2012*
Stochastic TDC

Ideal condition (no noise, no PVT)
Stochastic TDC

Noise & Process variation
threshold distribution

0/1 (random)
**Stochastic TDC**

Linearity compensation is potentially synthesizable and not very difficult.

Output code

\[ 0 \sim n - 1 \]

\[ t_0, t_{\text{start}} - t_{\text{stop}} \]

*P. M. Levine, et al., IEEE ITC 2004*
Pulse Injection

- Severe timing design is required on the injection pulse width.

*B. Helal, et al., JSSC 2009*
Measured Phase Noise

Frequency: 900MHz
Integrating Jitter: 1.7ps
\( P_{DC} \): 780\( \mu \)W

Phase Noise [dBc/Hz]

Offset Frequency [Hz]

10k 100k 1M 10M

-120
-80
-40
0
Simulated $C_{\text{medium}}$ against $V_{\text{in}}$

$D_{M}=1$

$D_{M}=0$

Miller effect

$C_{\text{medium}}$ [fF]

$V_{\text{in}}$ [V]

PMOS+offset

NMOS

offset
**Fine Varactor**

Miller effect is gain-dependent.

A transient variation of $V_{OUT}$ can make a fine capacitance difference in $C_{IN}$.

*W. Deng, et al., ISSCC 2014*
Fine Varactor (cont.)

Medium resolution

Fine resolution

*W. Deng, et al., ISSCC 2014
Robust for Layout Uncertainty

- Integrating Jitter: 1.7ps
  - \( P_{DC} = 780\mu W \)
  - FOM: -236.5 dB
- Integrating Jitter: 2.32ps
  - \( P_{DC} = 640\mu W \)
  - FOM: -234.6 dB

Fully synthesized (proposed)

Hierarchical P&R with synthesized DCOs (for comparison)