Anatomy of Innovation: Bug or Feature?

“Interpolation techniques” in ADCs

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Bug triggered to find the “interpolation”

I have failed to develop a sub-ranging ADC.
I had only Three weeks from idea to tape-out for the new ADC.
I founded the most robust ADC architecture; “Interpolation”

Compare the two signals (Reference is involved)
Free from the course-fine gain matching

Bug!!


US 5,151,700
The interpolation is not the equal division between the two voltages, but the internal division; weight and sum of the two values.

Many implementation methods are possible.
Invention of the capacitive interpolation

An ultra-Low FoM CMOS 10b ADC (1/8 to others) has been realized.

Capacitive interpolation
Chopper comparator
Pipelining


US 5,465,093

FoM of 10b ADC

FoM (pJ)

Out

Good DNL

Out

In

In

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Gate-width weighted interpolation

Gate-width can be used for the weighting

Array of gate-width weighted dynamic comparators with preamplifiers realizes high speed and low power ADC

Effective threshold voltage condition

\[ W_1 V_{o1} + W_2 V_{o2} > W_1 V_{o1} + W_2 V_{o2} \]

An ultra-low power (1/10 to others) and high speed ADC


But, no use for the interpolation

K. Sushihara, A. Matsuzawa, “A 7b 450MSample/s 50mW CMOS ADC in 0.3mm²,” ISSCC 2002.

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Conversion rate (Msps)
Position statement

• **Bugs** are always the **triggers** for innovative ideas.
  – unexpected bad result, a failure of development, a high pressure for development schedule, and tough performance targets

• The innovative ideas are **created from the logical thinking**. Seeking the **essence** of technology leads us to the novel view.
  – What is an analog to digital conversion?
  – Why a reference voltage is needed?
  – What is an interpolation?

• High level **abstraction** of the system, such as mathematical model sometimes **reveals the essence**. If we can find it, we can create many implementation methods easily.

• The other important factor is a **sense of beauty**. I believe an essential feature is always beautiful.