

Picosecond Resolution Time-to-Digital Converter Using G_m -C Integrator and SAR-ADC

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Abstract—A picosecond resolution time-to-digital converter (TDC) is presented. The resolution of a conventional delay chain TDC is limited by the delay of a logic buffer. Various types of recent TDCs are successful in breaking this limitation, but they require a significant calibration effort to achieve picosecond resolution with a sufficient linear range. To address these issues, we propose a simple method to break the resolution limitation without any calibration: a G_m -C integrator followed by a successive approximation register analog-to-digital converter (SAR-ADC). This translates the time interval into charge, and then the charge is quantized. A prototype chip was fabricated in 90nm CMOS. The measurement results reveal a 1 ps resolution, a -0.6/0.7 LSB differential nonlinearity (DNL), a -1.1/2.3 LSB integral nonlinearity (INL), and a 9-bit range. The measured 11.74 ps single-shot precision is caused by the noise of the integrator. We analyze the noise of the integrator and propose an improved front-end circuit to reduce this noise. The proposal is verified by simulations showing the maximum single-shot precision is less than 1 ps. The proposed front-end circuit can also diminish the mismatch effects.

Index Terms—Time-to-digital converter (TDC), time-of-flight (TOF), time interval measurement, time to amplitude conversion, G_m -C integrator, SAR-ADC

I. INTRODUCTION

A time interval measurement (TIM) module can be found in many time-of-flight (TOF) systems for industrial, medical and entertainment applications such as laser rangefinder, high-energy physics experiments, and 2D/3D imaging systems. Its main purpose is to quantize the time interval of a pulse signal or the time interval between the rising edges of two signals. The resolution of the time quantization is a key factor for the measurement accuracy. For example in a reflective TOF imaging system, a 1 mm resolution requires 6.7 ps minimum resolvable time. A high resolution also leads to a high signal-to-noise ratio (SNR) of the generated images.

The conceptual block diagram of a TIM module and its operation timing diagram is shown in Fig. 1. The measured time interval between Start and Stop contains integer (D_{int}) and fractional parts (D_{frac}). The integer part is the number of cycles

of a system clock CK_{sys} , which is measured by a counter gated by Start and Stop. The fractional parts (T_1 and T_2) are the time intervals that are not captured by the CK_{sys} . These fractional parts are quantized by a TDC. Generally, the resolution of the TDC determines the resolution and the accuracy of a TIM module. This paper focuses on the design and implementation of a high resolution TDC.

The most conventional TDC is realized with a delay chain [1] [2], as shown in Fig. 2, where CK_1 and CK_2 are two input pulses whose time difference T_{in} is quantized. Its resolution is limited to the delay of a logic buffer. In 90nm CMOS, such delay is around 20 ps, which is insufficient for resolving sub-millimeter level distance. Although higher resolution can be obtained by using more advanced process technologies; however, they are not always accessible for economic reasons and may pose design issues on other building blocks. Various architectures have recently been proposed to break this limitation, but a picosecond resolution TDC with sufficient linear range remains challenging. Vernier chain TDCs using two chains have been proposed [3]-[8]. The buffer delay in one chain differs from the one in the other so that the resolution becomes the subtraction of the two delays. However, the architecture is sensitive to the surges of supply voltage and temperature, thus a DLL loop is typically employed for a global calibration at the cost of power and area [3] [6] [8]. Despite of the supply voltage and temperature calibration, the effective resolution can potentially be undermined by the mismatches of buffers that are cumbersome to calibrate. Moreover, if a long chain is required for a large input range (such as 512 stages), jitter becomes an issue. Using short chains with time amplifiers (TA), a sub-range and a pipeline TDC have been proposed. Using TA to amplify the time residue for the next stage to quantize, this architecture achieves high resolution and long range. However, the nonlinearity and mismatches of TAs require tough calibration effort [9] [10]. To average out the effects of jitter, mismatch, and quantization noise, delta-sigma TDCs have been proposed using oversampling and noise-shaping techniques [11]-[14]. These approaches are only effective for the inputs with the time difference slowly changing, i.e. the input bandwidth is kept low (less than 3 MHz). On the other hand, the mismatch can be utilized by a stochastic TDC. It sums the results of a bunch of arbiters, whose mismatches are Gaussian, to form a transfer function. The resolution would be high, but the linear region of the transfer function is inherently short [15] [16]. The TDCs mentioned above break the resolution limitation, but they generally require

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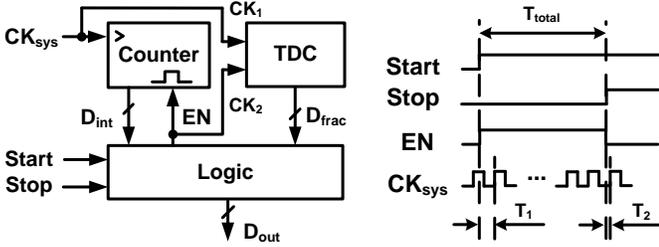


Fig. 1. Time interval measurement module and its operation timing diagram.

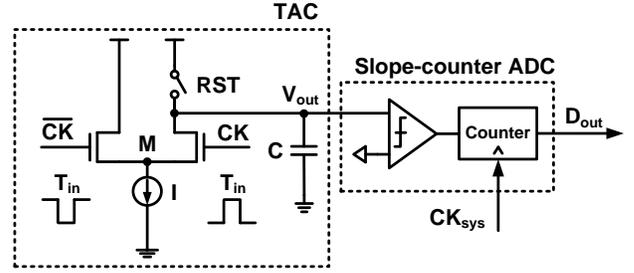


Fig. 4. Conventional TAC and ADC using switched current.

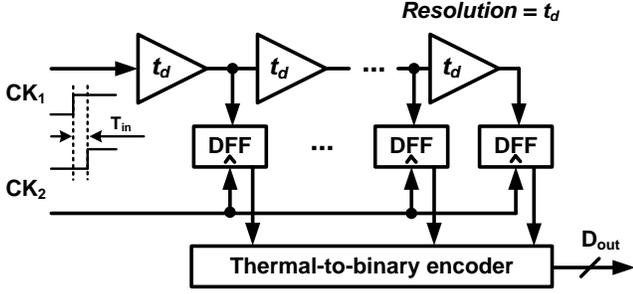


Fig. 2. Conceptual block diagram of delay-chain TDC. The resolution is limited by the delay of the buffer.

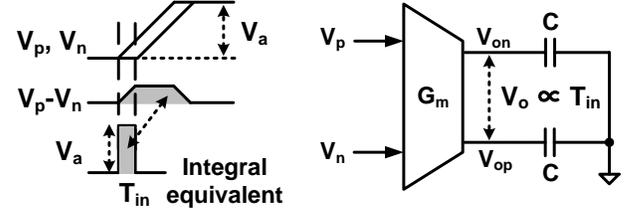


Fig. 5. Concept of proposed TAC using G_m -C integrator. The integral of $(V_p - V_n)$ is equivalent to the integral of an ideal pulse with amplitude V_a and pulse width T_{in} . The integrated voltage V_o is proportional to T_{in} .

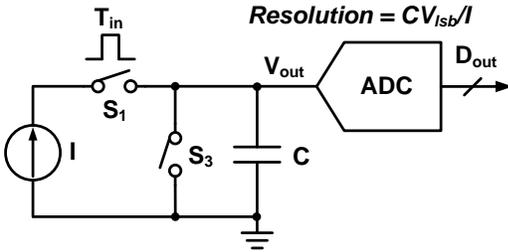


Fig. 3. Conceptual block diagram of TAC+ADC-based TDC. The resolution is potentially high using time-to-amplitude conversion.

a great amount of calibration effort.

The limited buffer delay as the fundamental issue of a delay chain TDC can be also circumvented using a time-to-amplitude converter (TAC) and an analog-to-digital converter (ADC). Reference [17]-[20] are a few examples of the TAC+ADC-based TDCs. The conceptual block diagram is shown in Fig. 3, where a stable current source is switched to charge a capacitor (via S_1), and the capacitor is reset at the end of each conversion (via S_3). The time difference T_{in} is translated into charge, which is quantized by the ADC afterward. The time resolution can be calculated with $t_{res} = CV_{lsb}/I$, where picosecond resolution can be easily obtained (e.g. $C = 1\text{ pF}$, $V_{lsb} = 1\text{ mV}$, $I = 1\text{ mA}$, $t_{res} = 1\text{ ps}$). However, the following issues have discouraged the deployment of this type of TDC: 1) the nonlinearity of the TAC, 2) the power consumption and the area of the ADC, and 3) the thermal noise and mismatches from the current source.

In this paper, we address these issues and present a TAC+ADC-based TDC with picosecond resolution. A chip solving the issues 1) and 2) was fabricated and measured [21].

A proposal solving issue 3) is given with analysis and simulation results. Section II introduces the concept and the architecture of the proposed TDC chip. Section III describes the circuit design of each building block. Section IV gives the measurement results of the fabricated chip. Section V proposes the potential improvement on thermal noise and the mismatch, with analysis and simulation results. Finally, Section VI draws the conclusion.

II. PROPOSED TDC

A. TAC Using G_m -C Integrator

A conventional TAC [19] [20] comprises of a current mode logic (CML) cell and a capacitor, as shown in Fig. 4, where RST is the switch to reset the capacitor at the end of each conversion. The slope-counter ADC will be discussed in the next subsection. The CML cell is switched by a pulse signal CK whose pulse width T_{in} is the time difference to be measured. The other branch controlled by CK is used to reset the voltage of node M to minimize charge sharing. Since the parasitic capacitance of the switch limits the rising/falling time of CK, which is generally tens of picosecond, an ideal pulse cannot be realized. A T_{in} shorter than the rising/falling time can degrade the linearity of the TAC due to the partially turned on switch. The use of a switch may also introduce charge injection and clock feed-through to degrade the linearity.

We propose a TAC using a G_m -C integrator to solve these issues. Its concept is shown in Fig. 5, where V_p and V_n are two input pulses with the amplitude V_a and time difference T_{in} . The integral of the subtraction of V_p and V_n , i.e. the shaded area, is equivalent to the area of the rectangle, $T_{in}V_a$; thus, (1) is obtained. Considering the circuit operation, the G_m cell generates a differential current proportional to the subtraction of V_p and V_n , and the current is integrated on the capacitor C, as

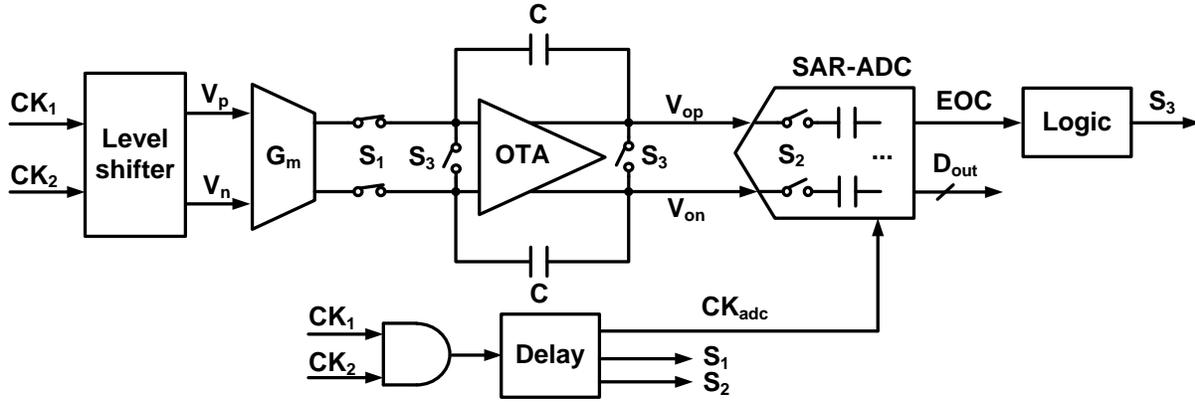


Fig. 6. Architecture of the proposed TDC.

shown in (2). Assuming the transconductance g_m is constant, which is generally reasonable with a small V_a , (3) can be derived. Thus, the time resolution is calculated with (4), where V_{lsb} is the minimum resolvable voltage. Interestingly, t_{res} is determined by the charge and a nominal current $-g_m V_a$. The integration stops when V_p equals V_n , due to the differential characteristic.

$$\int (V_p - V_n) dt = V_a \cdot T_{in} \quad (1)$$

$$\int g_m (V_p - V_n) dt = \int i_c dt = CV_o \quad (2)$$

$$V_a \cdot T_{in} = \frac{CV_o}{g_m} \quad (3)$$

$$t_{res} = \frac{CV_{lsb}}{g_m V_a} \quad (4)$$

The proposed TAC has two advantages leading to higher linearity: 1) the time difference is differentially integrated instead of using a pulse signal. Thus, even with a T_{in} smaller than the rising/falling time, the charge can be fully integrated. 2) No switches are involved in the differential integration. Although in actual circuits the correlation between g_m and V_a can degrade the linearity, the second-order nonlinearity is cancelled by the fully-differential structure, and the third-order one can be diminished by linearization techniques.

B. Selection of the ADC

A low-power and small-area ADC is required. Moderate conversion rate and resolution are acceptable. As shown in Fig. 4, a conventional work using a slope-counter ADC suffers from low speed. Furthermore, it requires an external counting clock CK_{sys} whose frequency affects the ADC's resolution and power consumption. A flash ADC is capable of extremely high speed with low resolution. To increase its resolution, the comparators increase exponentially so that significant power, area and calibration are involved. A pipeline ADC features high speed and high resolution. However, the amplifiers consume a significant amount of power and its architecture takes large area. A delta-sigma ADC suffers low speed though it features extremely high resolution. Since it contains integrators using operational amplifiers, high power and large area are also inevitable.

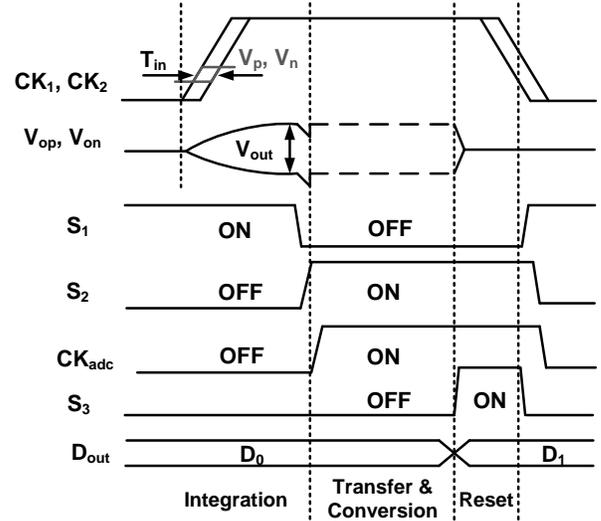


Fig. 7. Timing of the proposed TDC.

A SAR-ADC fits this TDC best. Unlike other types of ADCs, a SAR-ADC contains only one capacitive digital-to-analog converter (CDAC) for sampling and quantization, one comparator, and some small-scale logic circuits. Thus, low power consumption and small occupied area can be realized. By using metal-oxide-metal (MOM) capacitors and a dynamic comparator, the power consumption and occupied area can be further reduced while maintaining a moderate sampling rate [22]. Moreover, the binary-weighted CDAC suggests that the resolution can be scaled easily; the resolution can be increased by simply adding capacitors instead of the comparators or the op-amps that are required by other ADC architectures.

C. Architecture and Timing

The proposed architecture is shown in Fig. 6. A level shifter acts as an interface between the digital inputs and the G_m cell. An operational transconductance amplifier (OTA) is used to enhance the output resistance of the G_m cell. Switches S_1 and S_2 are used to control the sampling of the SAR-ADC. Switch S_3 resets the capacitor on each conversion cycle. The level shifter shifts the digital levels of CK_1 and CK_2 to the input common voltage with small amplitude to ensure a relative constant g_m . Only the differential input is integrated so that the integration

stops when both CK_1 and CK_2 reach high levels. After the integration, S_1 is turned off and S_2 is turned on. Since the feedback through the capacitor C still overrides the OTA, the output voltages of the OTA are held and copied to the sampling capacitors of the SAR-ADC. Then, CK_{adc} starts the analog-to-digital conversion. The conversion should end before the next rising edges of CK_1 and CK_2 . After that, S_3 is turned on to reset the capacitors and the converted data is output.

III. CIRCUITS DESIGN

A. Level Shifter

A capacitive level shifter without static current flow is proposed as shown in Fig. 8. Prior to the rising edges of the digital inputs CK_1 and CK_2 , V_p and V_n are preset to an input common mode voltage V_{init} . V_p and V_n have the amplitude V_a during the transitions of CK_1 and CK_2 . V_a is calculated with (5), where V_{dd} is the power supply voltage. When both CK_1 and CK_2 are low, V_p and V_n are reset to V_{init} .

$$V_a = \frac{C_1}{C_1 + C_2} V_{dd} \quad (5)$$

B. G_m -C Integrator

A conventional G_m cell and a gain-boostered folded-cascode OTA have been designed, as shown in Fig. 9, where S_1 to S_3 shown in Fig. 6 are omitted for a concise illustration. In the G_m cell, source degeneration and a relatively large effective gate voltage ($V_{gs} - V_{th}$) are used to increase the linearity. Since the inputs are not fully differentially driven by the level shifter, unbalanced charges are kicked back to the input. Neutralization transistors are used to alleviate this effect. Cascode current source is employed for a higher common-mode rejection ratio (CMRR). The voltage variation of the G_m cell is suppressed by the OTA with capacitive feedback so that its output resistance is increased. The current generated by the G_m cell is copied by the OTA and integrated on C . Boosting amplifiers A_1 and A_2 with folded-cascode structure are used to increase OTA's output resistance. The purpose of increasing the output resistances is to prevent the current leakage during the

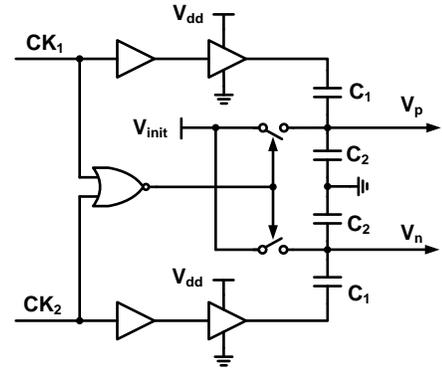


Fig. 8. Topology of the level shifter.

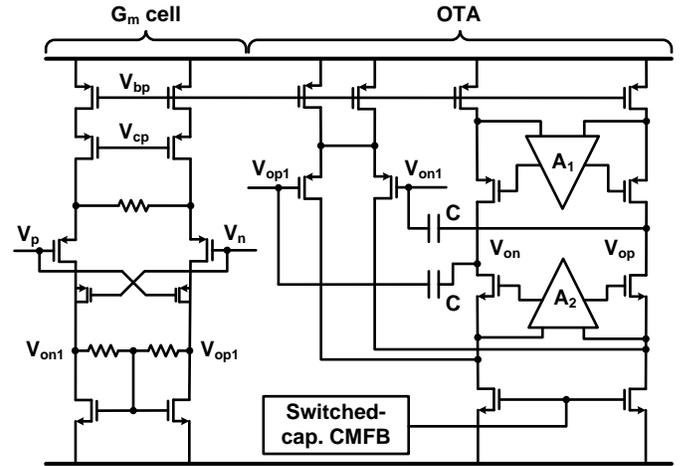


Fig. 9. Topology of the G_m -C integrator.

integration to enhance the linearity.

C. SAR-ADC

The topology of the SAR-ADC is shown in Fig. 10 (a). MOM capacitors are implemented due to its merit of high density and standard process, comparing with metal-insulator-metal (MIM) capacitors. Furthermore,

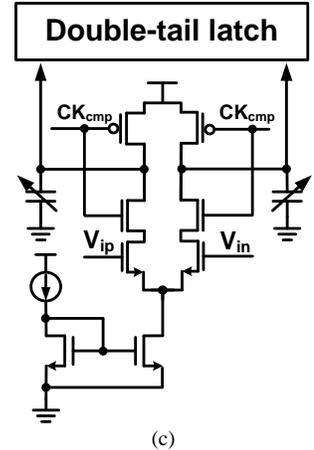
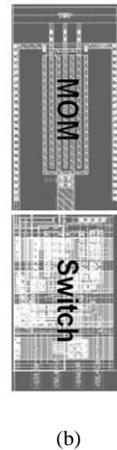
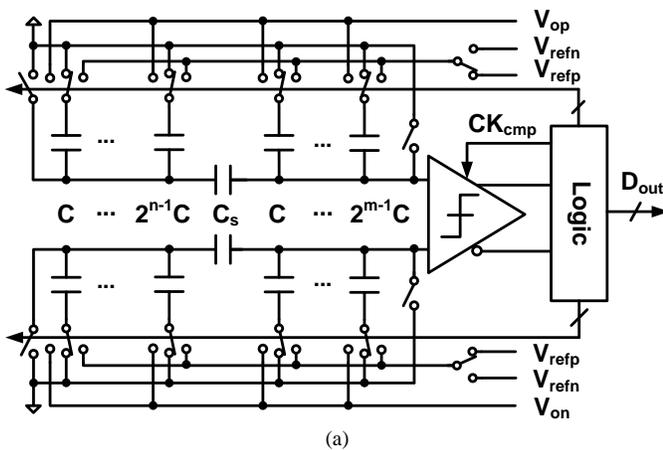


Fig. 10. (a) Topology of the SAR-ADC. (b) Capacitor-switch unit. (c) Topology of the dynamic comparator.

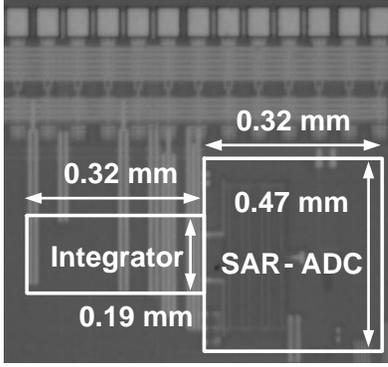


Fig. 11. Chip photo.

attributed to the finger-type structure, a MOM capacitor scales easily like a CMOS transistor. In addition, by maintaining the same pitch for the capacitor and the switch, they can be made into a capacitor-switch unit enhancing the matching of the CDAC. The layout of the capacitor-switch unit with 15 fF unit capacitance is shown in Fig. 10 (b). A dynamic comparator modified from [23] is designed without static current flow (except for the bias circuit), as shown in Fig. 10 (c). Hence, the entire SAR-ADC consumes only dynamic power, which allows its power consumption to scale with its sampling frequency.

IV. MEASUREMENT RESULTS

A prototype IC has been fabricated in 90 nm CMOS. The chip photo is shown in Fig. 11. The SAR-ADC has achieved 9.8-bit effective number of bits (ENOB) at 10 MS/s sampling rate, and 1 mW power consumption, and 0.15 mm^2 area occupation. Since the SAR-ADC is with 12-bit topology, if an actual 10-bit SAR-ADC is designed, the area of the SAR-ADC can be reduced to around 1/8. The core area of the integrator and the SAR-ADC are 0.06 mm^2 . With two 10 MHz input clocks acting as digital inputs and 1.2 V power supply, the total power consumption is 20.4 mW. Most of the power is consumed by the integrator due to the conventional static topology. It can be further reduced by optimizing the gain of the OTA and by power gating techniques.

To measure DNL and INL, two frequencies with nominal 40 Hz difference are input to the TDC creating a series of time

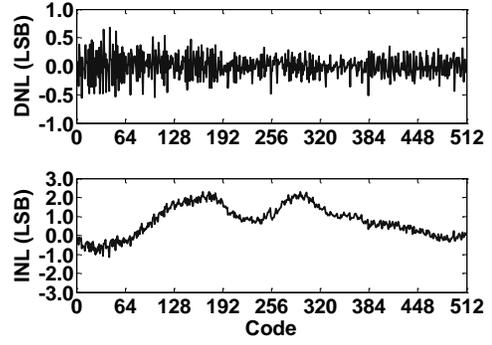


Fig. 12. Measured DNL and INL in 9-bit range with 1 ps per LSB.

ramps. Since the ENOB of the SAR-ADC is 9.8-bit, 10-bit output data are recorded by a logic analyzer. The histogram method was used to evaluate the DNL and INL. The result in the middle 9-bit is illustrated in Fig. 12, where DNL and INL are $-0.6/0.7 \text{ LSB}$ and $-1.1/2.3 \text{ LSB}$, respectively, with 1 ps per LSB. The measured performance is compared to other state-of-the-art TDCs in Table I, where the 1 ps resolution surpasses most of other works except for [10]. The performance of [10] is obtained after multi-step foreground calibration. When the operating environment has changed, the calibration may have to be performed again. In contrast, the performance of this work was obtained without any calibration, i.e. the proposed TDC achieves picosecond resolution while relieving the calibration effort. If the proposed TDC is used in a TOF rangefinder for 3D imaging, it would be possible to resolve 0.15 mm distance.

To evaluate the intrinsic noise, a single-shot precision test was carried out, which measured the standard deviation at the output of the TDC when a constant input time interval is applied. As shown in Fig. 13, a measured single-shot precision is 11.74 ps. Although averaging or oversampling can be used to reduce the noise, a periodic input with low bandwidth is required which is unavailable in some applications. We propose a method to reduce the intrinsic noise in the next section. This method also contributes to reducing the mismatch effects from the integrator.

TABLE I
PERFORMANCE COMPARISON

	JSSC'00 [19]	TCAS-I 10 [8]	TNS'12 [11]	TNS'07 [7]	VLSI 11 [10]	ESSCIRC'10 [15]	This work
Type	Switched-TAC	Vernier	Delta-sigma	Vernier	Pipeline	Stochastic	Integrator
CMOS (nm)	800 (BiCMOS)	180	130	130	130	65	90
Supply (V)	5	1.8	1.2	3.3	1.3	1.2	1.2
Resolution (ps)	32.0	14.6	6.0	37.5	0.63	3.0	1.0
Range (ps)	-	>50000	20000	2000	1300	52	± 256
DNL (LSBs)	-	0.7@1ns range	-	0.2	0.5	1.4	0.7
INL (LSBs)	-	0.8@1ns range	-	0.35	2	1.5	2.3
Area (mm^2)	11.9	0.33	0.11	0.22	0.32	0.04	0.31
Conversion rate (MS/s)	-	2	0.2	0.1	65	40	10
Power (mW)	-	6.4	1.7	150	10.5	8	20.4

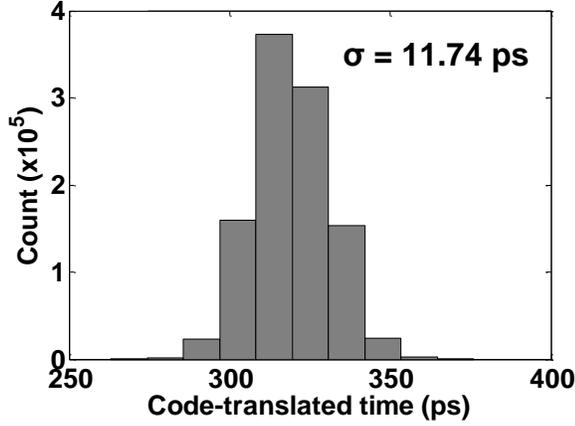


Fig. 13. Measured single-shot precision.

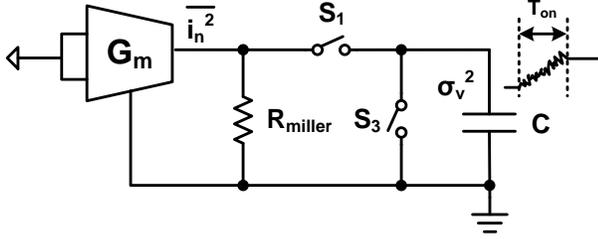


Fig. 14. Noise model of proposed TAC.

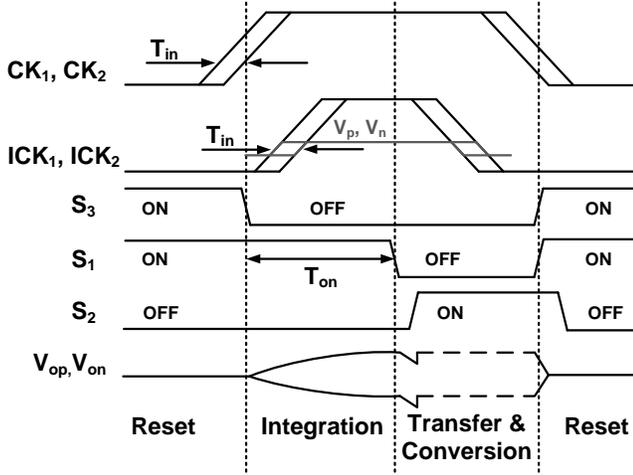


Fig. 15. Improved timing sequence to suppress the noise.

V. CIRCUITS IMPROVEMENT

A. On Single-Shot Precision

Intrinsic jitter and noise undermine the effective resolution of a TDC, especially when the resolution goes to picosecond scale. In this section, an improved front-end circuit is proposed to suppress the intrinsic noise to within 1 LSB (or 1 ps).

The single-shot precision in the proposed TDC is degraded by the jitter from the digital front-end circuits and the noises

TABLE II
EXAMPLE OF NOISE-AWARE PARAMETER DECISION

Parameter	Value
N	4
t_{res} (ps)	1
C (fF)	512
Resolution of ADC (bits)	10
V_{lsb} (uV)	977
g_m/I_d (S/A)	10
α	0.25
T_{on} (ps)	376
σ_v/V_{lsb}	0.5

from the switches, the OTA, and the G_m cell. By carefully sizing the input buffers and reducing the input digital chain as much as possible, the jitter effect can be mitigated. The noise from the switches can be also suppressed by using larger capacitors. Since the noise sources of the OTA sees a low-gain transfer function due to the feedback, compared with the noise from the G_m cell, the latter one is dominant.

The analysis model of this noise is shown in Fig. 14, where R_{miller} stands for the amplified (by the OTA) output resistance of the G_m cell so that a lossless integrator can be approximated. Considering the case when S_1 is on and S_3 is off, the noise of this lossless integrator has been analyzed in time domain [24] and in frequency domain [25] both leading to the same result. Fitting to our circuits, the noise from the G_m cell is calculated in (6), where N is the number of transistors dominating the noise assuming that their transconductances are the same, and T_{on} is the time interval during when signal and noise are integrated, i.e. the time during S_1 is on and S_3 is off.

$$\sigma_v^2 = N \cdot \frac{4kT\gamma g_m}{2C^2} \cdot T_{on} \quad (6)$$

Equation (6) can be rewritten into (7) where I_d is the bias current of the differential pair, α is the ratio of charging current over the bias current, g_m/I_d is a parameter for transistor sizing [26]. Therefore, the integrating capacitance, the time resolution, the ADC quantization step, the linearity of the G_m cell, and the integration time can be used to trade off with the noise. An example of the parameters is listed in Table II where the standard deviation at the output is half of the ADC's quantization step.

$$\frac{\sigma_v}{V_{lsb}} = \sqrt{N \cdot \frac{2kT\gamma}{CV_{lsb}} \cdot \frac{g_m}{\alpha I_d} \cdot \frac{T_{on}}{t_{res}}} \quad (7)$$

It can be seen that short T_{on} is important to suppress the integrated noise. Hence, the timing sequence shown in Fig. 7 is improved as in Fig. 15. Before the rising edges of the inputs, S_3 is on so that the integrator is reset and no noise from the G_m cell is integrated. When either CK_1 or CK_2 rises, S_3 is turned off, followed by the rising edge of the delayed input ICK_1 or ICK_2 . The integration starts when S_3 is turned off. After T_{on} , the output voltages should be settled, and S_1 is turned off to stop the noise integration. S_1 triggers S_2 to transfer the settled voltages to the SAR-ADC. The sequence afterwards is same as in Fig. 6 except that ICK_1 and ICK_2 fall after T_{on} because they are

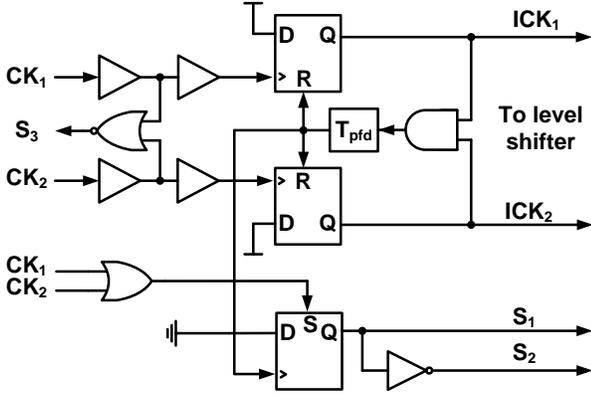


Fig. 16. Improved front-end circuit to suppress the noise.

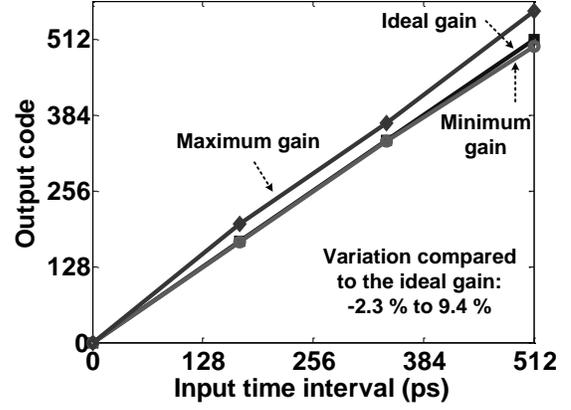


Fig. 19. Gain variation due to the mismatch in the G_m cell.

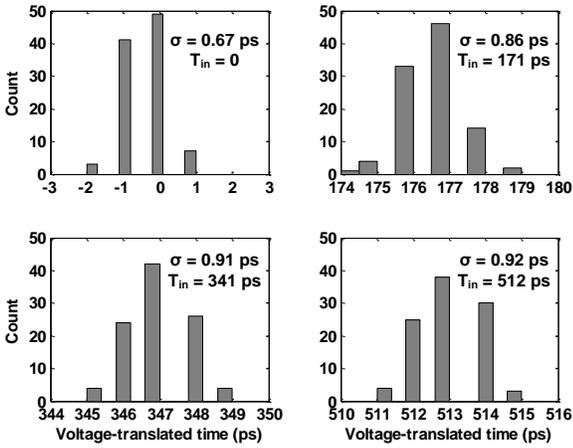


Fig. 17. Simulated single-shot precisions of the improved TAC.

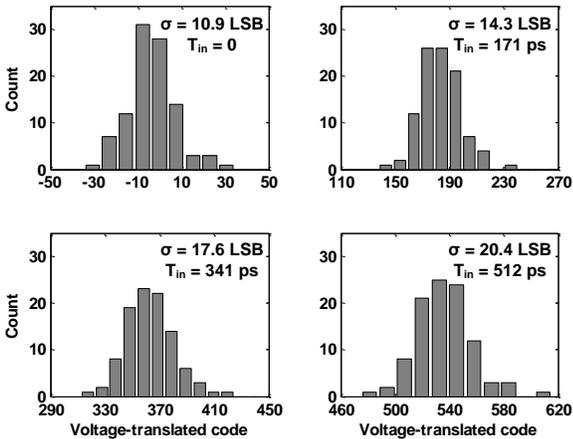


Fig. 18. Monte-Carlo simulation of the output offsets of the improved TAC.

generated by a phase frequency detector (PFD) shown in Fig. 16. Fig. 16 also shows the circuits to control S_1 to S_3 . Sufficient T_{on} is needed to cover the settling time of V_{op} and V_{on} . Although the settling time can be calculated in a numeric way, which is

basically the inverse Laplace transform, circuit simulation is still required so that an iterative design flow is needed.

A TAC with the improved front-end circuit as shown in Fig. 16 is designed using the parameters listed in Table II. With different input time intervals (T_{in}), the differential voltages transferred to the ADC's sampling capacitors are simulated. These voltages are translated into time, and their distributions are shown in Fig. 17. Since T_{on} depends on the input time interval and must cover the settling time of the TAC, shortest T_{on} in this design is 100 ps longer than the required one in Table II. Consequently, the single-shot precision is more than 0.5 LSB and increases with the input time interval. Other noise sources such as timing jitters and switches also contribute to the noise. Nevertheless, single-shot precisions less than 1 LSB or 1 ps can be achieved.

B. On Mismatch Effects

The mismatch of the TAC can generate a DC voltage offset. Similar as the noise effect, the mismatch in the G_m cell is dominant since the DC voltage is amplified by the OTA and accumulated on the capacitors. A short T_{on} is thus also important to attenuate the offset. With the improved design mentioned in the previous sub-section, a Monte-Carlo simulation of the voltage transferred to the ADC is performed. The voltage is translated into the digital code as shown in Fig. 18. The standard deviation of the DC-offset 10.9 LSBs is observed when T_{in} is zero. This offset can be easily subtracted from the digital output in a data processing block.

The mismatch in the G_m cell also leads to different transconductances of the input transistor pair. The charge error caused by the different transconductances is calculated in (8), where g_{m1} and g_{m2} are the two different transconductances in the transistor pair. Equation (8) shows a proportional relation with input time interval, which corresponds to Fig. 18 where with 512 ps input time interval, the mean output code is around 540. The increase of the standard deviation is also due to this effect. Consequently, the gain or resolution of the TDC varies with each set of the mismatch.

$$\Delta Q = (g_{m1} - g_{m2}) \cdot V_i \cdot T_{in} \quad (8)$$

The gain variation can be quantified with the data used in Fig. 18. Since the Monte-Carlo algorithm is indeed pseudorandom in the simulator, the left boundary bins represent the same seed of the mismatch, and vice versa to the right ones. Hence, the gain variation can be plotted as shown in Fig. 19 using boundary bins subtracting the corresponding ones in the subfigure where T_{in} is zero (this subtraction cancels out the DC-offset). The gain varies from -2.3 % to 9.4 % compared to the ideal one, suggesting the resolution varies from 0.98 ps to 1.09 ps. This variation is negligible in most applications.

VI. CONCLUSION

We have presented a TAC+ADC-based TDC achieving picosecond resolution. Conventional issues of such TDCs are the nonlinearity of the TAC, the high power and large area of the ADC, and the thermal noise from the TAC. This paper provides solutions to the issues by proposing a G_m -C-based TAC for linear integration, a SAR-ADC for low power and small area, and an improved front-end circuit to reduce the noise. The former two solutions were verified through chip measurement while the latter one was verified via simulation. A prototype IC was fabricated in 90 nm CMOS. The measured DNL and INL are -0.6/0.7 LSB and -1.1/2.3 LSB, respectively, with 1ps per LSB in a 9-bit range. The measured power and area are 20.4 mW at 10 MHz rate and 0.31 mm², respectively. Although the measured single-shot precision is 11.74 ps, we have analyzed the noise and provided a possible solution. The noise analysis shows that reducing the integration time reduces the intrinsic noise and mismatch effects. The simulation confirms that our proposed front-end circuit can realize single-shot precision of less than 1 ps, a DC-offset which can be digitally cancelled, and negligible resolution variation. Compared with state-of-art TDCs, our proposal achieves picosecond resolution without calibrations.

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