A Pulse-Driven LC-VCO with a Figure-of-Merit of -192dBc/Hz

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***Abstract*—This paper proposes a LC-VCO with a pulse-driven cross-coupled pair. The proposed pulse driving technique has the ability to achieve class-C like current waveform while reducing the Amplitude-Modulation to Phase-Modulation (AM-PM) conversion by parasitic capacitance of the active devices. A VCO is implemented using the proposed technique in a standard 0.18um CMOS technology. It oscillates at a carrier frequency of 3.6GHz with a 0.65-V supply. The measured phase noise is -124 dBc/Hz @ 1MHz-offset with a power consumption of 2.05mW. The figure-of-merit (FoM) is -192 dBc/Hz.**

I. Introduction

Rapid advancements in the digital base-band systems demands high performance low power solution for their high frequency wireless links. One of the main components that directly influence the transceiver in terms of both power consumption and performance is the Voltage Controlled Oscillator (VCO) used in them. Because of this reason, VCO's with extremely good phase noise and very low power consumption are highly sought after nowadays. LC-VCO is one of the oscillator topologies that has the capability to surpass the tough performance metrics required by emerging wireless communication standards.

When discussing about LC-VCO, one cannot avoid mentioning Class-C VCO, which has been one of the major breakthroughs in the VCO designs and has ever since been the norm for evaluating new designs. However, the necessity to keep the transistors in saturation region for successful class-C operation imposed a minimum limit on the achievable phase noise and it also introduced start-up issues. Researchers [2] [3] [4] successfully solved these issue by introducing adaptive bias schemes for the cross-coupled pair.

In this work, we investigate the affects of driving the cross-coupled pair of an LC VCO with a very low voltage. The analysis reveals a phase noise degradation phenomenon that results from the non-linear nature of the parasitic-capacitance introduced by the large devices used as the cross-coupled pair. The degradation in phase noise is more pronounced when the cross-coupled pair is operated with low overdrive voltage. This work also proposes a solution to this problem by exploiting the time-variant nature of the VCO.

This paper is organized as follows: section II briefly reviews the conventional class-C VCO and states the importance of operating the cross-coupled pair in saturation region. This section also presents the issues when the transistors are operated in weak saturation region. Section III explains the proposed pulse driving technique and its advantages over the conventional way of biasing the cross-coupled pair with a constant voltage. This section also contains the design details of the proposed VCO. Section IV gives the measurement results and the conclusions are made in section VI.

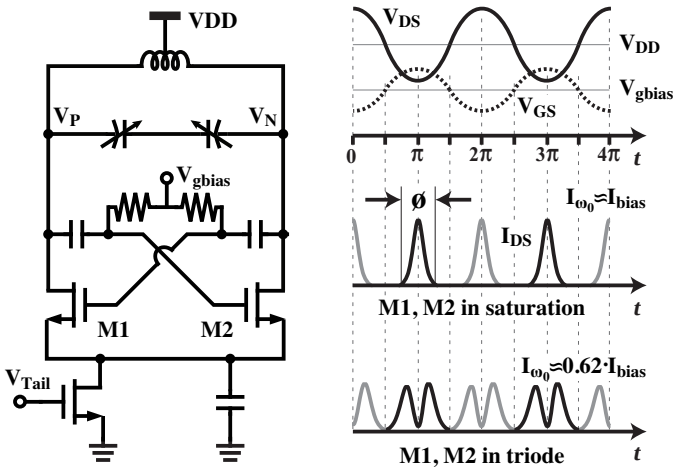

Fig. 1. Conventional class-C VCO and relevant voltage and current waveforms.

II. Conventional class-C VCO: A brief review

Fig. 1 shows a class-C VCO circuit topology along with the current and voltage waveform of the tank and the gate of cross-coupled pair. Class-C operation is achieved in this design by isolating the bias of M1 and M2 from the tank and providing a lower voltage. It can be seen from the figure that this results in a reduction of conduction angle and an improvement in current efficiency in comparison with conventional class-B LC-VCO. The analysis done by [1] revealed a considerable degradation in current amplitude when the transistors are operated in deep triode region rather than in saturation region. This reduction in current amplitude directly impacts the phase noise performance of the VCO. Because of this reason, for a conventional class-C VCO, it is vitally important to bind the operating region of the cross-coupled transistors within cut-off and saturation. For ensuring excellent phase noise, the DC-bias voltage of the cross-coupled pair must be set very close to or lower than the threshold voltage of the transistors,

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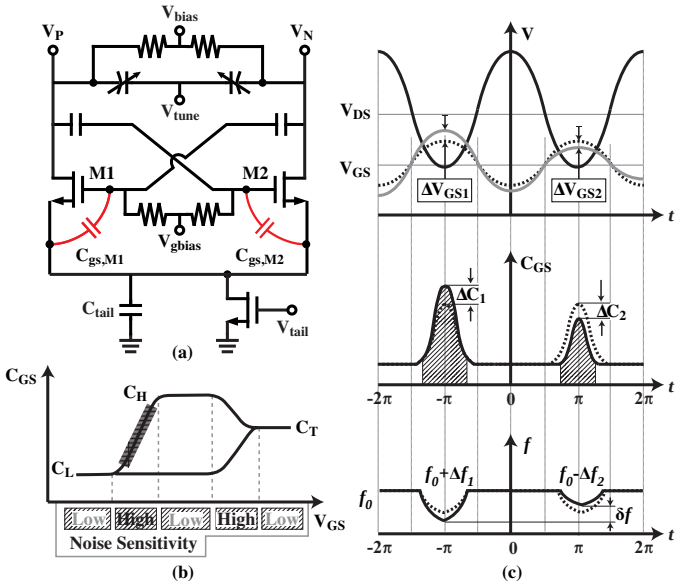

Fig. 2. (a) Conventional class-C VCO topology showing gate-to-source capacitance ($C_{\rm gs}$) (b) variation in gate-to-source capacitance ($C_{\rm gs}$) over gate-to-source voltage($V_{\rm gs}$) (c) AM-PM conversion due to the non-linear characteristics of $C_{\rm gs}$.

which enhances the maximum headroom for the tank signal. But setting such low bias voltages introduces serious start-up issues.

The problem of biasing the cross-coupled pair without introducing any start-up issues was solved by a number of innovative designs [2] [4] [3]. The basic principle involved in most of these designs is to start the oscillator in class-B mode and gradually bring down the DC-bias of the cross-coupled transistors so that the DC-operating point is shifted to class-C region. When such self-biasing schemes are employed, the overdrive voltage of the cross-coupled pair becomes extremely low. It is necessary to have a large transistor to ensure unrestricted current flow at these low overdrive voltages. Large transistors also help in reducing the conduction angle. When large transistors are employed in the design, the parasitic capacitance introduced by them can no longer be neglected and must be taken into account while analyzing the circuit.

Fig. 2 analyzes the effects of the large gate-to-source capacitance ($C_{\rm gs}$) on the phase noise performance of the system. Fig. 2(b) shows the variation in ($C_{\rm gs}$) with respect to the gate-to-source voltage ($V_{\rm gs}$). When $V_{\rm gs}$ of the transistor is below threshold voltage ($V_{\rm th}$), the capacitance is $C_{\rm L}$. When the transistor is driven into heavy saturation region (with large enough $V_{\rm ds}$), the capacitance saturates at $C_{\rm H}$. A similar condition occurs in deep triode region, where the junction capacitance saturates at $C_{\rm T}$. It can be observed from Fig. 2(b) that during the transitional state from cut-off to saturation and from cut-off to triode, $C_{\rm gs}$ has a linear relationship with $V_{\rm gs}$. From the above discussions, it can be deduced that, for optimum performance, the overdrive voltage of a class-C VCO has to be in the transitional region between the cut-off and saturation-as shown by the shaded region of Fig. 2(b)). Fig. 2(c) shows the adverse effects of operating the transistor in this region.

It is evident from Fig. 2(b) that any change in the gate voltage results in a variation in $C_{\rm gs}$ which translates to a shift in the instantaneous frequency. This instantaneous frequency shift will degrade the overall phase noise of the system. Ideal conditions are represented in Fig. 2(c) by dotted lines where as the conditions under the presence of noise is shown by solid lines. It must be observed that for the instantaneous frequency to be constant, the amplitudes of $V_{\rm gs}$ as well as $V_{\rm ds}$ must remain constant. This AM-PM conversion cannot be neglected in conventional class-C design since there are a number of implicit and explicit reasons for aforementioned amplitude variations. From Fig. 2(a), some of the explicit noise sources are the noise up-converted from the tail-transistor and the noise coupled from the supply lines and from varactor bias. Another issue of conventional class-C VCO is squegging. Even though squegging can be minimized to a certain extend with good design, there is still a possibility for small amounts of squegging in the manufactured device. Even these negligible variations in the amplitude will be magnified by the large change in $C_{\rm gs}$.

III. Proposed Pulse-Driving Technique

A. The Concept

Conventional way of biasing a class-C VCO is shown in Fig. 3(a). From the discussion given in the previous session, the issue of applying a low voltage at $V_{\rm gbias}$ is evident. Fig. 3(b) shows a simplified model of the proposed pulse-driven bias scheme for the cross-coupled pair. Instead of applying a constant bias voltage, the proposed pulse-driven

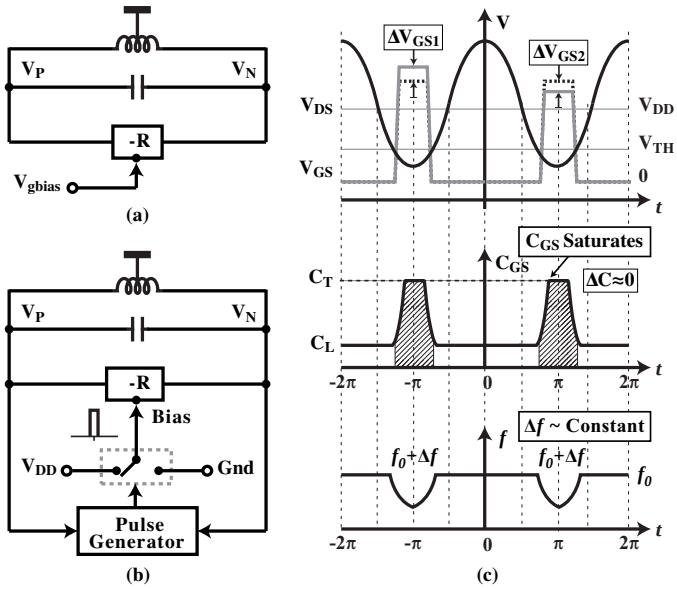

Fig. 3. Conceptual diagrams showing bias mechanism of (a) conventinal class-C and (b) proposed pulse-driven bias scheme (c) suppression of AM-PM conversion by driving transistors into deep-triode.

bias technique produces pulses that are synchronized to the oscillator and use these pulses for switching the DC-bias between a HIGH (VDD) and a LOW (GND) voltage levels. It can be seen that varying the width of the pulse can control the conduction angle of the transistor. For a given frequency of oscillations, varying the pulse width using this method can change the DC-operating point. Careful consideration reveals that using this technique, all modes of operations ranging from class-A to class-C can be achieved. If the pulses are kept small enough, the oscillator works in class-C and it has the potential to achieve the excellent phase noise performance guaranteed by the impulse like current shaping property of class-C oscillators. Also, since the voltage level is changed as in a digital circuitry, the transistors will be either in cut-off or in deep-triode region. The advantages of allowing the transistors into the triode region is two fold, (i) tank oscillations are no longer limited by the saturation conditions that needs to be satisfied in the conventional class-C design. (ii) AM-PM conversion phenomenon discussed in the previous section has less effect when $V_{\rm gs}$ is kept high. This can be understood by observing Fig. 2(b) and Fig. 3(c). A high enough $V_{\rm gs}$ results in saturation of the gate-to-source capacitance ($C_{\rm gs}$). Since the capacitance is bound to saturate in this bias scheme, any change in the amplitude of $V_{\rm gs}$ and $V_{\rm ds}$ has less effect on the instantaneous frequency.

Another advantage of the proposed pulse-driven bias scheme can be understood by observing Fig.4. Since the pulse used for the bias is completely isolated from the tank, superposition principle must be used for evaluating the effective amount of voltage applied to the cross-coupled transistor. If designed carefully, the feedback factor (k) can be made greater than one. Any improvement in k directly translates to an improvement in phase noise [1].

B. The Proposed VCO using Pulse-Driven Bias Technique

Fig. 5 shows the complete circuit diagram of the VCO employing pulse-driven cross-coupled pair. This design solves the challenge of achieving a low conduction angle while maintaining the overdrive voltage of the cross-coupled pair at a sufficiently high value. The main differences between the conventional class-C and the proposed design can be observed as the replacement of the constant (or adaptive bias schemes)

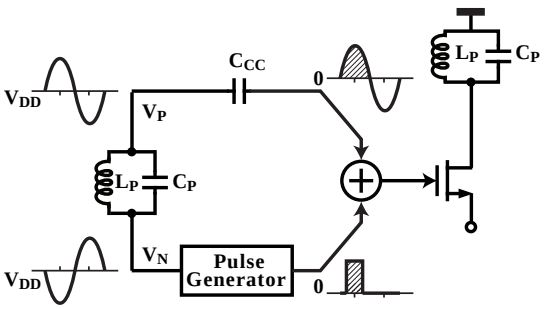

Fig. 4. Feedback enhancement by voltage superposition.

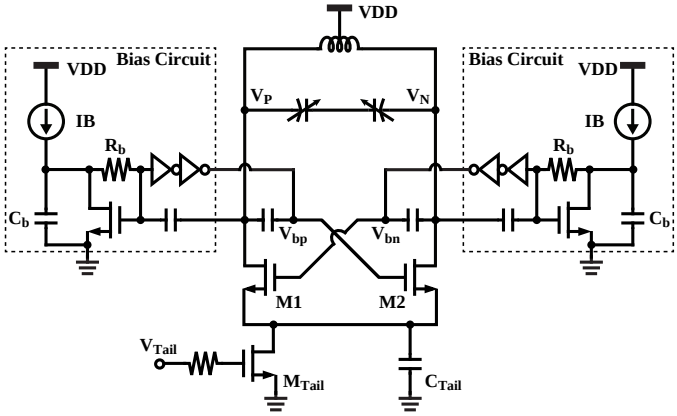

Fig. 5. Circuit schematic of proposed pulse-driven VCO.

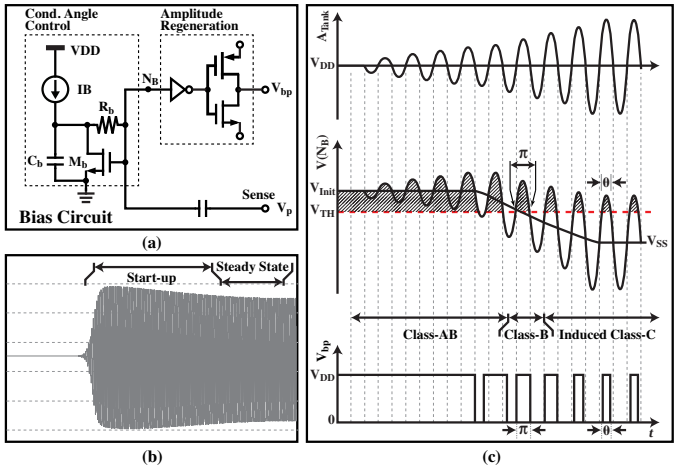

Fig. 6. (a) Detaied circuit schematic of the bias network (b) simulated output voltage of the proposed oscillator (c) graphical anaysis of the proposed pulse-driven bias mechanism.

that are used in the conventional topology for biasing the cross-coupled pair by a pulse based bias circuit.

The circuit used for realizing the pulse-driving scheme for the cross-coupled pair proposed in the previous section is shown in Fig. 6(a). The bias circuit consists of two blocks, (i) conduction angle control unit and (ii) Amplitude regeneration unit. Function of the conduction angle control unit is to enforce a low conduction angle after ensuring a robust start-up. The amplitude regeneration network brings the voltage level to an acceptable level in order to drive the transistors of the cross-coupled pair into deep-triode region.

Fig. 6(b) explains the working of the pulse-driven bias circuit with the help of relevant waveforms. $A_{\rm tank}$ represents the oscillations in the tank. $V(N_{\rm B})$ and $V_{\rm bp}$ represents voltage at the input of amplitude regeneration network and the output of the bias network respectively. The working of this bias circuit can be broken down into four separate regions for easiness of understanding. (i) When the oscillator is in the start-up phase and the oscillations are below the threshold voltage level $V_{\rm th}$, node $N_{\rm B}$ is kept above the threshold value by the bias current

I_B flowing in the conduction angle control network. As a result, $V_{\rm bp}$ is switched to HIGH. During this, the oscillator works in class-A mode and ensures a very robust start-up against wide PVT variations. (ii) As the oscillations builds up and starts crossing $V_{\rm th}$, transistor $M_{\rm b}$ in the conduction angle control module starts turning ON. This averages the current flowing in the capacitor $C_{\rm b}$ and brings down the DC-voltage coupled at node $N_{\rm b}$. Thus, the bias control network gradually start to traverse from class-A to class-B mode through class-AB. (iii) Class-B mode is achieved when the DC-bias at node $N_{\rm b}$ reaches $V_{\rm th}$. (iv) After this point, further reduction in the DC-bias at $N_{\rm b}$ forces the conduction angle to assume a value that is less than π. and hence drives the oscillator into class-C mode. The amplitude reduction observed in the conventional class-C is avoided in this work by forcing the transistor into cut-off everywhere beyond the conduction region. Fig. 6(c) shows the simulated voltage waveform at the output node of the proposed VCO. It also depicts the start-up and steady state conditions. With careful design of the proposed bias circuit, it is possible to obtain steady state oscillations as shown in Fig. 6(c), where the oscillator behavior is similar to that of class-C oscillators.

IV. Measurement Results

The VCO using the pulse-driven cross-coupled pair shown in Fig. 5 is fabricated in a standard 180nm CMOS process. The core chip area is $500\mu\text{m} \times 310\mu\text{m}$. For comparison purposes, a conventional class-C VCO with similar dimensions is also fabricated on the same die. The VCO using the proposed pulse-driving technique achieved a phase noise of -124dBc/Hz@1Mhz offset from a carrier of 3.6GHz carrier with a power consumption of 2.05mW, including the bias circuitry from a supply voltage of 0.65V. Corresponding FoM is evaluated at -192dBc/Hz. Whereas the reference class-C VCO achieved a FoM of -190dBc/Hz with a power consumption of 2.54mA from 0.65V supply voltage while operating at similar bias conditions. The measurement data showed a noticeable improvement in the FoM validating the proposed theory.

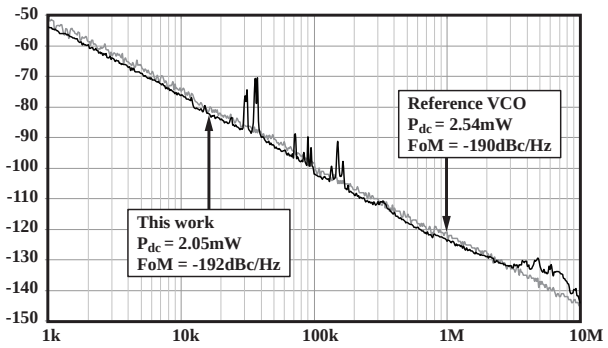

Fig. 7. Measured phase noise of the reference VCO and propsed VCO.

TABLE I
Comparison of pulse-driven VCO with state-of-the-art VCOs.

	CMOS Process	Frequency [GHz]	Phase Noise [dBc/Hz]	$P_{\rm dc}$ [mW]	FoM [dBc/Hz]
[1]	130nm	4.9	-130@1MHz	1.3	-196
[2]	180nm	4.5	-109@1MHz	0.16	-190
[3]	180nm	4.84	-125@1MHz	3.4	-193
[4]	90nm	5.1	-120@1MHz	0.86	-192
[5]	65nm	3.7	-142@3MHz	15	-192
[6]	65nm	4.8	-144@10MHz	4.0	-191
This work	180nm	3.6	-124@1MHz	2.05	-192

V. Conclusion

This paper briefly analyses the AM-PM conversion mechanism due to the non-linear nature of gate-to-source capacitance that results in a degradation of phase noise performance. A VCO design using pulse-drive technique is proposed as a solution. If carefully designed, it has the potential to considerably improve the performance of LC-tanlk oscillators.

Acknowledgment

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References

[1] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE Journal of Solid-State Circuits*, vol.43, no.12, pp.2716-2729, Dec. 2008.

[2] K. Okada, *et al.*, "A 0.114mW dual-coduction class-C CMOS VCO with 0.2-V power supply," *IEEE symp. VLSI Circuits (VLSIC)*, pp.228-229, Jun 2009.

[3] Wei Deng, K. Okada and A. Matsuzawa, "Class-C VCO With Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing," *IEEE Journal of Solid-State Circuits)*, vol.48, no.2, pp. 429-440, Feb 2013.

[4] M. Tohidian, *et al.*, "High swing class-C VCO," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp.495-498, Sep. 2011.

[5] M. Babaie and R. B. Staszewski, "A Class-F CMOS Oscillator," *IEEE Journal of Solid-State Circuits*, vol.48, no.12, pp.3120-3133, Dec. 2013.

[6] L. Fanori and P. Andreani, "Class-D CMOS Oscillators," *IEEE Journal of Solid-State Circuits*, vol.48, no.12, pp.3105-3119, Dec. 2013.

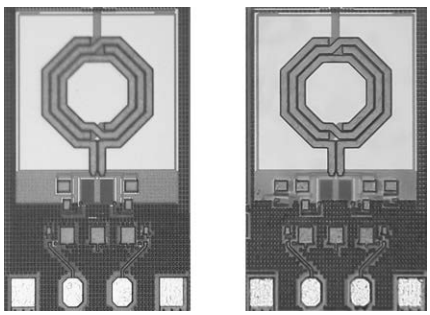

Fig. 8. Chip micrograph of reference VCO (left) and proposed VCO (right).