This paper proposes a dual-loop injection-locked PLL with synthesizable all-digital PVT calibration system for SoC clock generation[1]. This circuit is implemented in a standard 65nm CMOS technology. The die micrograph is shown in Fig.1. The measured phase noise maps to a 0.7 ps jitter when integrated from 10 kHz to 40 MHz. The proposed dual-loop ILPLL has an operating range of 0.5-to-1.6 GHz, and it consumes a total power consumption of 0.97 mW excluding output buffer, from a 1 V power supply. The measured reference spur is ~57 dBc. The reference clock can be varied from 40 to 300 MHz. All the above-mentioned measurements are performed at the room temperature.