Applying for: [ ] Category I  [ ] Category II  [ ] Category III

Research topic: A 60-GHz CMOS Direct-Conversion Wireless Transceiver

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Expected graduation year/month: 2013/March  Nationality: Japan

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- The purpose of this research

Recently, high-speed wireless communication at 60GHz is attracted. This is because the very wide bandwidth around 60GHz can be used without license in many countries, and high speed wireless communications can be realized such as 40Gb/s in 64QAM modulation. Represented by rapid advance of smartphones, high data rate wireless communication is required more and more. Thus our target is to realize 60GHz ultra high-speed wireless communication.

- The manner and degree this research advances the science and/or technology

The research advance is to realize practical applications of 60GHz wireless communication. 60GHz is assumed to use in short range and to set up on mobile instruments such as smartphones. To realize practical use, many issues should be solved such as realization of 16QAM, power consumption, chip area. In our research, CMOS 65nm process and direct-conversion architecture are employed considering these issues. As a result, ultra low-power 60GHz CMOS transceiver has been realized.

- Specific results that have been obtained and their significance

In our research, lower-power and higher-integration 60GHz CMOS transceiver is implemented. It is the world-first 4channels 16QAM 60GHz CMOS transceiver. Up to now, no one can achieve 60GHz wireless communication in all channels. Moreover, our transceiver achieves 16Gb/s data rate which is world-best record in 60GHz. It is to get closer to realize practical applications of 60GHz that high data rate and low-power transceiver is achieved simultaneously.
Dear Sir/Madam

Ryo Minami is one of our recommending students. He received a B.E. degree in Electrical and Electronic Engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2011. He is studying toward his M.E. and Ph.D. degrees in Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan.

I had several opportunities to observe his performance. Being his teacher of Analog RF circuit experiments, I first became acquainted with him about 2 years ago, and since then I have enjoyed ample opportunity to observe his many talents. Thus I feel that I can evaluate him very well in terms of engineer and personality.

Our research group is working on research and development of RF CMOS front-end for mmW wireless communication. In our research group, he designed the receiver of mmW wireless transceiver in master 1st and the performance of transceiver is presented in ISSCC 2011 and 2012.

Up to now, our 60GHz transceiver has issues in relation to conversion gain flatness. Gain flatness is significantly affected the EVM(Error Vector Magnitude), especially for a single-carrier system. According to IEEE standard, 9GHz bandwidth is released around 60GHz and that is separated into 4 channels. To realize 16QAM for every channel, we need to suppress gain flatness under 2dB. He made efforts to solve this issue. He designed equalizing amplifier to compensate gain degradation and gain flatness was suppressed under 1dB for every channel. Thus we can achieve high data rate, which is 7.04Gb/s, for every channel and achieved world best EVM. In addition, the maximum rate can be extended up to 16Gb/s, which is the limit of measurement equipment.

As for his personality, first of all, as mentioned above, he has been proved to be hard-working and initiative. For example, last summer vacation, he almost spent all his time at school, doing research, measurement, analysis, and help for my presentation of ISSCC2012. Moreover he has made efforts to improve the performance of RF transceivers for next target. He designed some effective circuit component and technique for 60GHz transceivers, and these were presented in famous international conferences.

Not only research and development, but also he pays great attention to the study of languages and cultures. He is very active to present in foreign countries, so I strongly recommend him for TSMC outstanding student research award. I can give more information if requested.

Kind regards,

Research Advisor

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(Abstract)

Due to the explosive increase of data traffic, a higher data rate is also required for wireless communication. Recently, the technologies using 60-GHz carrier frequency have been remarkable. According to IEEE802.15.3c standard, four 2.16-GHz-bandwidth channels around the 60GHz are defined and 3.5Gb/s in QPSK and 7Gb/s in 16QAM modulation can be achieved. This is the big motivation to use the 60GHz carrier frequency.

Fig.1 shows the entire block diagram of the 60-GHz RF front-end. The RF chip is implemented using a 65nm CMOS process. The transmitter (Tx) consists of a 4-stage PA in Fig.2, differential preamplifiers, I/Q double-balanced Gilbert mixers, as shown in Fig.3, and a quadrature injection-locked oscillator(QILO). In this work, a transmission-line based design is employed because the length of layout components cannot be ignored as compared with the wavelength. Moreover, capacitive cross-coupling technique is used to improve max gain and reverse isolation. The receiver (Rx) consists of a 4-stage LNA in Fig.4, differential amplifiers, I/Q passive mixers, a QILO, and baseband amplifiers in Fig.5. As gain is degraded accompany with the increasing of baseband (BB) frequency, BB amplifier can compensate the gain degradation by using gain peaking technique. In addition, this Rx can realize variable gain by using the gate bias adjustment. Each amplifier has a wideband matching for covering the four channels defined in the 60GHz wireless standards.

Fig.6 shows the measured Tx conversion gain and power characteristics. Tx covers 4 channels and saturated output power of ch.3 is 6dBm. Moreover, LO leakage and sideband rejection ratio are more than 40dB for every channel. Fig.7 shows the measured Rx conversion gain and noise figure (NF). Gain flatness of the Rx is suppressed under 1dB for every channel because of gain peaking technique of the BB amplifier. The measured NF of ch.3 is less than 4.9 dB, which is the best performance as a 60-GHz CMOS receiver. Fig.8 shows the measured output power and IM3. IIP3 of Rx is -14dBm in a low gain mode.

The 60GHz QILO as shown in Fig.9 works as a frequency tripler with an integrated 20GHz PLL, and generates center frequency of each channel with a 36MHz reference. For a 60-GHz oscillator, this 7-GHz frequency tuning range cannot easily be covered. In addition, there is a trade-off between the phase noise and the frequency tuning range, and at least -90dBc/Hz phase noise should be realized for 60-GHz direct conversion transceivers. Fig.10 and Fig.11 show the output spectrum of the QILO and measured phase noise. Due to the injection-locked technique, phase noise of the 60-GHz QILO is determined by the 20-GHz PLL. Since the quality factor of on-chip inductors and capacitors is still high at 20GHz, we can realize good phase noise and wide tuning range at 60GHz. In this work, we can obtain a phase noise of less than -95dBc/Hz at 1-MHz offset frequency for every channel.

Figs.12 and 13 show die photo of the RF chip and measurement setup. An arbitrary waveform generator is used to generate a modulated signal and a digital oscilloscope is also used to evaluate the modulation performance. The RF chip is implemented in a BGA package and 6-dBi antennas embedded in the package for Tx and Rx. Table I shows the summary of measurement results for 16QAM, showing the constellation, spectrum, back-off, RF data rate, EVM, SNR(MER), and communication distance. The symbol rate is 1.76Gs/s with a roll-off factor of 25%, and the RF data rates with 2.16 GHz-BW is 7.04Gb/s for 16QAM. The EVM measurement is around -23dB for every channel, which is normalized by the maximum symbol amplitude. The maximum communication distance is about 1.6m in QPSK, and 0.5m in 16QAM. An improved version is also implemented, and it achieves 16Gb/s with a wider bandwidth in 16QAM.

The transmitter and receiver consume 257 mW and 162 mW from a 1.2-V supply, respectively. The PLL consumes 61 mW. Considering the communication in QPSK only, Tx and Rx consume 150 mW and 104 mW, respectively.

Table II shows a performance comparison. The proposed RF transceiver integrates Tx, Rx, LO including PLL, and is evaluated with the embedded antennas. This RF front-end covers all channel of 60-GHz and achieves full-data rates for QPSK and 16QAM with the best EVM, moreover compared with other one, low power transceiver is achieved.
Fig. 1. Block diagram of the 60-GHz direct-conversion transceiver.

Fig. 2. 60-GHz 4-stage power amplifier.

Fig. 3. Up-conversion mixer.

Fig. 4. 60-GHz 4-stage low noise amplifier.

Fig. 5. Down-conversion mixer.

Fig. 6. Tx conversion gain and output power.

Fig. 7. Rx conversion gain and NF.

Fig. 8. Rx output power.
Fig. 9. Quadrature injection locked oscillator.

![Quadrature injection locked oscillator](image)

(a) free-run
(b) injected

Fig. 10. Output spectrum of the QILO.

![Output spectrum](image)

Fig. 11. Measured phase noise of the 60GHz LO.

![Phase noise measurement](image)

Table I. Measurement result for 16QAM.

<table>
<thead>
<tr>
<th>Channel</th>
<th>ch. 1</th>
<th>ch. 2</th>
<th>ch. 3</th>
<th>ch. 4</th>
<th>Max rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constellation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spectrum</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Back-off</td>
<td>4.4 dB</td>
<td>4.6 dB</td>
<td>5.0 dB</td>
<td>5.7 dB</td>
<td>5.0 dB (ch. 3)</td>
</tr>
<tr>
<td>Data rate</td>
<td>7.0 Gb/s</td>
<td>7.0 Gb/s</td>
<td>7.0 Gb/s</td>
<td>7.0 Gb/s</td>
<td>10.0 Gb/s (ch. 3)</td>
</tr>
<tr>
<td>EVM</td>
<td>-23.0 dB</td>
<td>-23.0 dB</td>
<td>-23.3 dB</td>
<td>-22.8 dB</td>
<td>-23.0 dB (ch. 3)</td>
</tr>
<tr>
<td>SNR</td>
<td>20.4 dB</td>
<td>20.5 dB</td>
<td>20.7 dB</td>
<td>20.3 dB</td>
<td>20.4 dB (ch. 3)</td>
</tr>
<tr>
<td>Distance</td>
<td>0.3 m</td>
<td>0.5 m</td>
<td>0.5 m</td>
<td>0.3 m</td>
<td>&gt;0.01 m (ch. 3)</td>
</tr>
</tbody>
</table>

Table II. Performance comparison.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Max. rate in 16QAM</th>
<th>Distance for BER &lt;10^{-3}</th>
<th>P_Dc (Tx/Rx)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tokyo Tech [1]</td>
<td>11Gb/s [1] 16Gb/s [2]</td>
<td>ch.1-2 (EVM &lt; -17dB) 2.7m (BPSK/QPSK) 0.2m (BPSK/16QAM)</td>
<td>252mW / 172mW</td>
</tr>
<tr>
<td>Silbeam [3]</td>
<td>7Gb/s</td>
<td>ch.2-3 (EVM &lt; -19dB) 50m (LOS) 16m (NLOS)</td>
<td>1.820mW / 1.250mW</td>
</tr>
<tr>
<td>IMIC [4]</td>
<td>7Gb/s</td>
<td>ch.1-4 (EVM &lt; -17dB) (not wireless)</td>
<td>176mW / 112mW (w/o 20GHz PLL)</td>
</tr>
<tr>
<td>This work</td>
<td>10Gb/s</td>
<td>ch.1-4 (EVM &lt; -23dB) 1.3-1.6m (QPSK) 0.3-0.5m (16QAM)</td>
<td>319mW / 223mW</td>
</tr>
</tbody>
</table>