A 60GHz PVT-tolerant Injection-locked Frequency Synthesizer with a Background Frequency Calibration Technique

東京工業大学 理工学研究科, ○ティーラショート シリブラーノン, ウェイ デン, アハマド ムサ, 岡田 健一, 松澤 昭

東京工業大学, ○ティーラショート シリブラーノン, ウェイ デン, アハマド ムサ, 岡田 健一, 松澤 昭

tee@ssc.pe.titech.ac.jp

A 58.1-to-65.0 GHz frequency synthesizer using sub-harmonic injection-locking technique with background frequency calibration technique for Time Division Duplex (TDD) transceivers [1]-[2] is presented. The synthesizer is capable of supporting all 60GHz channels which are specified by IEEE 802.11.3c, wirelessHD, IEEE 802.11ad, WiGig, and ECMA-387 for short-range high-speed wireless communications. A frequency calibration scheme is proposed to monitor a frequency shift of quadrature injection locked oscillators which is caused by environmental variations. The proposed synthesizer is implemented in a 12-metal 65nm CMOS process, the synthesizer achieves a phase noise of -96 dBC/Hz @1MHz offset from a carrier frequency of 61.56 GHz.
