Proposing

An Interpolated Pipeline ADC

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Background

38GHz long range mm-wave system
Role of long range mm-wave

Current
- Optical fiber
- Base stations for WiFi and WiMAX
- Not flexible

Future
- Optical fiber
- Connect with mm-wave
- Very flexible
38GHz long range mm-wave system

realized 1Gbps long range mm-wave systems

Current system: 80Mbps!!
System configuration

Compatible with Gbit Ethernet
Hole system is integrated with planar antenna
A mixed signal SoC has been developed to realize 64QAM (1Gbps) with BW of 260MHz.

Co-developed with JRC
Developed ADC

Developed new 10b ADC to address 64 QAM.

Interpolated pipeline scheme
No need of high gain OP amps

Suitable for low gain and low V_{DD} scaled CMOS

10b, 320 MSps, 40mW ADC

BER vs. SNR

BER for 64QAM has been reduced to the ideal

ENOB of ADC is increased
Tokyo Tech. Model Network

Ten mm-wave base stations in our campus

Tokyo Tech. O-Okayama Campus
Expand the area to NEC (4km)

Challenge for 4km mm-wave communication
Outline

• Introduction
• Interpolation Techniques
• Circuit Implementation
• Measurement Results
• Conclusions
Conventional Pipelined ADC

Conventional pipelined ADC requires accurate MDAC
Pipelined ADC Conversion

\[ V_{o1} = 2 \left( V_{in} - \frac{1}{2} V_{FS} \right) \]

\[ V_{o2} = 2V_{o1} \]

\[ V_{o3} = 2 \left( V_{o2} - \frac{1}{2} V_{FS} \right) \]

Residue
\[
\begin{align*}
V_{in} & \quad V_{o1} \\
0 & \quad 1 \quad 0 \rightarrow 1 \\
\frac{1}{4} V_{FS} & \quad 0 \quad 0 \rightarrow 0 \\
\frac{1}{2} V_{FS} & \quad 0 \\
\frac{3}{4} V_{FS} & \quad 0 \\
V_{FS} & \quad 0
\end{align*}
\]

Output CODE
\[
\begin{align*}
1 & \\
0 \rightarrow 1 & \\
1 \rightarrow 0 & \\
13
\end{align*}
\]
Conventional MDAC

- High DC gain OpAmp
  - Difficult to realize in scaled technology
- Closed-loop MDAC leads to lower speed

\[
G_0 (\text{dB}) > 6N + 10
\]

\[
\text{GBW} > NF_s
\]

\[N: \text{Number of bits}\]

\[F_s: \text{Sampling freq.}\]
OpAmp gain and conversion error

\[
\varepsilon_{(\text{LSB})} = \frac{3 \times 2^N}{G} \quad G > \frac{3 \times 2^N}{\varepsilon_{(\text{LSB})}}
\]

\[G > 6N + 10 \text{ (dB)}\]

Gain>70dB

10bit ADC

Large error occurs

40dB gain
Recent Works

• Digital compensation technique [1, 2]
  – Capacitor mismatch, gain error and opamp nonlinearity can be corrected
    • Simple analog circuit design
  – Foreground compensation
    • PVT variation degrade the performance
  – Long compensation time
    • Increase of test cost

Proposed ADC

• Target: 10bit, $F_s > 300$ MS/s

• Interpolation and pipelined operation
  – Moderate relative gain
    • $\Delta G/G < 5\%$ for 10bit
    • Open-loop amplifiers can be used
    • No need of linearity compensation
  – Insensitive to settling time
    • High speed
    • Low power
Interpolation Architecture

\[ V_{oa} \rightarrow \text{Interpolator} \rightarrow \text{CMP} \]

\[ V_{ob} \]

\[ V_{out} \]

\[ V_{oa} \]

\[ V_{ob} \]

\[ V_{in} \]

\[ \text{CMP} \]
Interpolation Architecture

\[ V_{out} \]

\[ V_{oa} \]

\[ V_{ob} \]

Interpolator example [3,4]

Interpolation Architecture

Conversion error is not occurred by changing gain.
Interpolated Pipeline ADC Structure

Interpolation technique is used for 2-4th stage. Each stage has an 1-bit redundancy.

1st stage  2nd stage  3rd stage  4th stage

1st stage
- Pipeline Stage
- Sample & CDAC
- CMP1
- A1a
- Int. Caps.
- D1st (3b+1b)

2nd stage
- Pipeline Stage
- A1b
- Int. Caps.
- CMP2
- A2a
- D2nd (2b+1b)

3rd stage
- Pipeline Stage
- A2b
- D3rd (2b+1b)

4th stage
- Pipeline Stage
- D4th (2b+1b)
- D5th (1b)

Correction Logic

10b
Interpolation methods

- Static current
- Good linearity
- Imbalance settling

- No static current
- \( C_p \) causes nonlinearity

- No static current
- Good linearity
- Heavy load

Resistive (Series) [3,4]

Capacitive (Series)

Capacitive (Weighted)

Ex. 3bit

1:8
2:6
3:5
8:1

Total: 36Cu

\( A_{1a} \)

\( A_{1b} \)

\( V_{in} \)

\( C_p \)

\( C_{ua1} \)

\( C_{ub1} \)

\( C_u \)

\( C_{uaN} \)

\( C_{ubN} \)
Proposed Weight Controlled Capacitor Array

Sub-ADC controls the capacitor weight. Load capacitance is reduced from $36C_u$ to $16C_u$ (3bit).

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Weight Controlled Capacitor Array

Offset voltage can be cancelled in interpolation phase

\[
V_x = - \left[ \frac{m}{m+n} G_a (V_{\text{in}} - V_{\text{ra}}) + \frac{n}{m+n} G_b (V_{\text{in}} - V_{\text{rb}}) \right]
\]

\[2^M = m+n\]

\[
V_{oa} = G_a (V_{\text{in}} - V_{\text{ra}} - V_{\text{off}_a})
\]
\[
V_{ob} = G_b (V_{\text{in}} - V_{\text{rb}} - V_{\text{off}_b})
\]
\[
V'_{oa} = G_a (-V_{\text{off}_a})
\]
\[
V'_{ob} = G_b (-V_{\text{off}_b})
\]

\(G_a, G_b\): Gain of \(A_{1a}\) and \(A_{1b}\)

\(V_{oa}, V_{ob}\): Output voltage

\(V_{\text{off}_a}, V_{\text{off}_b}\): Offset voltage

\(V_{\text{ra}}, V_{\text{rb}}\): Reference voltage

\(m, n\): Capacitor weight
Interpolated Output

Interpolation phase

1bit redundancy

Interpolated Output

Interpolation phase

1bit redundancy
Sub-ADC Structure

Gate-width-weighted interpolation comparators with capacitive offset calibration is used.

– Offset voltage < 2 mV ($\sigma$)

Requirements for An Amplifier

• Absolute Gain error ⇒ No error
• Offset voltage ⇒ DNL error
  – Offset voltage < 1LSB
    • Offset voltage can be neglected by output offset cancel technique.
• Gain mismatch ⇒ DNL error
• Linearity ⇒ DNL and INL error
Amplifier : Schematic

1st stage amplifier require good linearity

=> CMOS input with source degenerations

Gain mismatch < 2.1%(3σ)
Amplifiers: Simulation results

\[ V_{out} \approx a_1 V_{in} - a_3 V_{in}^3 \]

1st stage \( a_3/a_1 < 1.3 \)
2nd stage \( a_3/a_1 < 6.2 \)

Gain [dB]

2nd stage amplifier
1st stage amplifier

Gain [dB]

2nd stage amplifier
1st stage amplifier

\( f_{3dB} = 1.2 \text{GHz} \)
\( C_{load} = 320 \text{ fF} \)

Output voltage vs. DC gain.

Frequency vs. gain.
Gain matching requirement

Gain mismatch of 1st stage amplifiers < 2.1%(3s)
Linearity Requirement

1st stage $a_3/a_1 < 1.3$, 2nd stage $a_3/a_1 < 6.2$

$V_{out} \approx a_1 V_{in} - a_3 V_{in}^3$
Chip photo

- 90 nm 10M1P CMOS technology
- Chip area of 0.46mm²
This periodical error is due to bad layout, not essential issue.
Sampling Frequency vs. SNDR

Input Frequency = 1 MHz

![Graph showing SFDR and SNDR vs. Fs (MS/s)]

- SFDR
- SNDR
Input Frequency vs. SNDR

Sampling Frequency = 320 MS/s
# Performance summary

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[2]</th>
<th>[6]</th>
<th>[7]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (bit)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>$F_{sample}$ (MS/s)</td>
<td>320</td>
<td>500</td>
<td>205</td>
<td>320</td>
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<tr>
<td>$V_{DD}$ (V)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.0</td>
<td>-</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>40</td>
<td>55</td>
<td>61</td>
<td>42</td>
</tr>
<tr>
<td>$\text{ENOB}_{\text{peak}}$ (bit)</td>
<td>8.5</td>
<td>8.5</td>
<td>8.7</td>
<td>8.7</td>
</tr>
<tr>
<td>$\text{FoM}<em>{F_s}/\text{FoM}</em>{ERBW}$ (pJ/c.-s)</td>
<td>0.35 / 0.77</td>
<td>0.31</td>
<td>0.65</td>
<td>0.36 / 0.44</td>
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<tr>
<td>Technology (nm)</td>
<td>90</td>
<td>90</td>
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<td>90</td>
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<tr>
<td>Active Area (mm$^2$)</td>
<td>0.46</td>
<td>0.5</td>
<td>1</td>
<td>0.21</td>
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<tr>
<td>Amplifier type</td>
<td>Open</td>
<td>Closed</td>
<td>Closed</td>
<td>Closed</td>
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<tr>
<td>Linearity Compensation</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Conclusions

• An interpolated pipelined ADC using open-loop amplifier has been proposed.
  – Interpolation architecture
    • $\Delta G/G < 5\%$ for 10bit
    • Using simple open-loop amplifiers enables high speed operation
    • No need of a linearity compensation
  – Weight Controlled Capacitor Array
    • Load capacitance is reduced from $36C_u$ to $16C_u$
    • Offset voltage of the amplifier can be cancelled
  – 10bit, 320MS/s, 40 mW ADC has been realized
Future Prospect

• Issue: Need twice larger circuits
  – Same capacitance as for the conventional pipeline ADC can be used by modifying circuits.
  – Area and power can be reduced, since lower bandwidth is acceptable.

• Still need the pipelined ADC?
  – SAR ADC: lowest FoM, but low $f_s$ and low resolution.
  – SAR-Pipeline: higher resolution, but lower $f_s$ due to multi step conversions.
  – Interleaving: effective for low resolution ADC, but need totally large capacitance.