n-Channel Metal–Oxide–Semiconductor Field-Effect Transistor Modeling in Forward Body Bias Condition for Low Voltage Complementary Metal–Oxide–Semiconductor Circuits Design

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This paper proposes a modified transistor model to improve the accuracy under the forward body bias operation that is vital for low voltage circuits, such as 0.5 V, to reduce the power consumption of complementary metal–oxide–semiconductor (CMOS) LSI. The proposed model and equations were implemented in BSIM4 version 4.6 with SPICE3f5 and verified by measurements of 60 nm n-channel metal–oxide–semiconductor field-effect transistors (n-MOSFETs). Approximately 50% inaccuracy of the drain current can be corrected. Furthermore, the importance of the proposed model will become higher with further lower threshold voltage operation requirements.

1. Introduction

In order to reduce power dissipation while maintaining speed of any circuits in battery supplied portable systems, the importance of low voltage sub-100 nm complementary metal–oxide–semiconductor (CMOS) technology is increasing.1) An effective approach to operate metal–oxide–semiconductor field-effect transistors (MOSFETs) at low bias voltages is a forward body-biasing scheme for extending bulk-Si CMOS technology scaling. A forward body bias improves threshold voltage roll-off behavior and enables the use of shorter gates, as explained by a quasi-two-dimensional (2D) model.2)

To simulate circuits with the forward body-biasing scheme, the MOSFET model is the key to reproduce the effect3–5) accurately. However, there are two major problems to characterize n-MOSFETs. One is the threshold voltages of n-MOSFETs that cannot be monotonically scaled whereas p-MOSFETs can. The other is the bulk charge which is mainly affected in the velocity saturation region.

During our circuit design process, we found that the existing MOSFET compact models, including BSIM36,4,7) and HiSIM2,8) do not make sufficient attention to the forward body bias operations. In particular the simulated drain current of n-MOSFET by the circuit simulator is much lower than the measured value under the forward body bias condition. So far, existing sub-micron MOSFET models including HiSIM2, BSIM4, PSP,9) and EKV310) describe the drain current formulation only under null and reverse body biases. An empirical equation of threshold voltage for forward body biases is written only in BSIM4 model source code.7) It is needed to develop a physical based model to simulate drain current in forward body biases in addition to null and forward body bias operations with sufficient accuracies.

We first formulate depletion thickness \((X_d)\) which is dominant to determine the threshold voltage \((V_{TH})\) using vertical and horizontal doping profiles. Next the bulk charge effect dependencies on reverse to forward body biases are analyzed and modeled. Then, these results are implemented into BSIM4 as an instance for simulating drain current from reverse to forward body bias ranges. Finally, the model is compared with measurement of 60 nm n-MOS transistors.

2. Modeling

2.1 Threshold voltage

As shown in Fig. 1, non-uniform doping profiles can be categorized into vertical non-uniformity and lateral non-uniformity.11) The vertical non-uniformity can be due to additional implantation for threshold voltage adjustment or for punch through prevention.12–14) On the other hand, lateral non-uniformity due to the intended pocket implantation for deep sub-micron technology or the unavoidable transient enhanced diffusion of boron impurity at the edge of the source and drain regions in n-MOSFET. Doping profiles of these two regions are modeled as Gaussian distribution.11)

We focus on the device operation in triode mode whose energy band diagrams are shown in Fig. 2. In the reverse body biasing condition, the conduction energy band has been bended to the amount of body bias. Accordingly, \(X_d\) becomes thicker than that of null body bias condition. When positive bias is supplied to the bulk, the energy band is slightly bended because the gate-to-source voltage \((V_{GS})\) is higher than bulk-to-source voltage \((V_{BS})\). Therefore, \(X_d\) is thinner than that of reverse and null body bias conditions. The forward body bias operation can also be explained by ionization mechanism which is illustrated in Fig. 1. It means

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Fig. 1. Cross-sectional diagram of a pocket n-MOSFET structure in the state of forward body biases. Inset illustration shows the ionization mechanism when the forward body bias was supplied.
that some percentage of channel electrons are ionized by the holes which are supplied by the bulk terminal. As a result, depletion thickness becomes smaller than that of null and reverse body biases. It is clear that $X_d$ is dominated by concentration of channel ($N_{ch}$) and pocket implant ($N_{pocket}$).

Since the forward bias reduces $X_d$, $V_{TH}$ has a strong dependency on $V_{BS}$, which is dominated by pocket implant. The forward $V_{BS}$ dependency of $X_d$ can be written as a non-uniform vertical doping model in

$$X_d = \frac{2 \varepsilon_f}{q N_{eff}} \cdot (\phi_S - V_{BS}). \tag{1}$$

Here, $\varepsilon_f$ is a dielectric constant of silicon, $\phi_S$ is the surface potential, $q$ is an electric charge. Effective channel carrier concentration ($N_{eff}$) is solved by

$$N_{eff} = 2 \int_0^{L_{PD}} N_{PD} \, dy + \int_{L_{PD}}^{L_{ND}} N_{NP} \, dy. \tag{2}$$

Here, $N_{PD}$ and $N_{PS}$ are drain and source carrier density, respectively, and $N_{NP}$ is the bulk density. As also shown in Fig. 3. $L_B$ is the standard deviation length of source (drain) carrier, $L_{PS}$ and $L_{PD}$ are the variance length of source and drain carrier, respectively. $L_{ND}$ is the unaffected bulk area length, and $L_{eff}$ is the effective channel length.

The drain channel density which is affected by surface state density ($N_{SS}$) and $N_{pocket}$ is written by

$$N_{PD} = \int_0^{L_{PD}} \frac{[N_{SS} + N_{pocket} \cdot \exp(-y/L)^2)] \, dy}{L_{PD}}. \tag{3}$$

Since the vertical doping profile of drain and source regions show Gaussian distribution, statistical functions can be used as shown in Fig. 3. $\sigma$ represents the standard deviation, $\sigma^2$ means the variance. Using Gaussian distribution calculation referred to Fig. 3, eq. (3) can be solved by

$$N_{PD} = \frac{\sqrt{\pi} \cdot l_p \cdot N_{pocket} \cdot erf \left( \frac{L_{PD}}{l_p} \right) + N_{SS} \cdot L_{PD}}{L_{PD}}$$

Here, erf is the error function encountered in integrating the normal distribution (which is a normalized form of the Gaussian function). In the same manner, $N_{PS}$ is represented by

$$N_{PS} = \frac{\sqrt{\pi} \cdot l_p \cdot N_{pocket} \cdot \frac{l_p}{L_{PS}} \cdot erf \left( \frac{L_{PS}}{l_p} \right) + N_{SS}}{L_{PS}}. \tag{4}$$

Assuming of drain and source channel as symmetrical, $L_{NP} = L_{eff} - L_{PD} - L_{PS}, L_{PD} = L_{PS} = \frac{l_p}{2}, N_{PD} = N_{PS},$ and $N_{NP} = N_{SS}$.

By plugging eqs. (4) and (5) into eq. (2), $N_{eff}$ is formulated as

$$N_{eff} = \frac{2 \cdot L_{PD} \cdot N_{PD} + L_{ND} - N_{NP} \cdot L_{PD}}{L_{eff}}. \tag{6}$$

Surface potential is written as

$$\phi_S = \phi_{S0} - \Delta \phi_S. \tag{7}$$

Here, $\phi_{S0}$ is the surface potential at $V_{BS} = 0$ and expressed as

$$\phi_{S0} = \frac{2kT}{q} \cdot \log \left( \frac{N_{eff}}{n_i} \right). \tag{8}$$

$\Delta \phi_S$ is written as

$$\Delta \phi_S = \phi_{DIBL} + \phi_{BF}. \tag{9}$$

$\phi_{DIBL}$ means the potential of drain induced barrier lowering (DIBL) and written as

$$\phi_{DIBL} = \lambda \cdot V_{DS}. \tag{10}$$

$\lambda$ is the DIBL coefficient. $\phi_{BF}$ is the potential drop which is mentioned earlier in Figs. 1 and 2. Since $\phi_{BF}$ is in proportional to forward $V_{BS}$ ($V_{BF}$), it is written as

$$\phi_{BF} = \lambda_B \cdot V_{BF}. \tag{11}$$

Here, $\lambda_B$ is the coefficient of forward body bias.
2.2 Saturation drain current
Unlike threshold voltage equations, most MOSFET compact models use variety types of empirical formulations to represent second order effects in drain current equations. In this research BSIM4 has been adopted for implementing forward body biasing effects.

A coefficient of bulk charge effect ($A_{\text{bulk}}$) which is a part of the saturation drain current ($I_{\text{DS}}$) in eq. (12) of BSIM4\(^7\) represents body biasing effects as shown in eq. (13):

$$I_{\text{DS}} = W C_{\text{ox}} (V_{\text{gs}} - A_{\text{bulk}} V_{\text{th}}) V_{\text{sat}}.$$  \hspace{1cm} (12)

$$A_{\text{bulk}} = \frac{1}{1 + K_{\text{eta}} V_{\text{th}}}.$$ \hspace{1cm} (13)

Here $V_{\text{sat}}$ is the velocity saturation.

$A_{\text{bulk}}$ was calculated and plotted from measured and simulated data using model equations in Fig. 4. The target n-MOSFET device, whose drawn channel length and width are 60 nm and 10 \(\mu\)m, respectively, for the measurement was selected from MOSFET TEGs using 60 nm CMOS technology. The $V_{\text{gs}}$ dependencies of $A_{\text{bulk}}$ in eq. (13) can only express proportionality relation in BSIM4 that needs to be modified to represent forward $V_{\text{th}}$ case. We empirically developed eq. (14) to express the reduction of $A_{\text{bulk}}$ at the forward body biases.

$$A_{\text{bulk}} = \frac{1}{1 + (K_{\text{eta}} + K_{\text{etavb}}) e^{V_{\text{th}}}}.$$ \hspace{1cm} (14)

Here, $W$, $C_{\text{ox}}$, $V_{\text{gs}}$, and $V_{\text{th}}$, are the channel width, oxide capacitance, $V_{\text{gs}}$ minus $V_{\text{th}}$, and saturation voltage, respectively. $F_{\text{dope}}$, $F_{\text{length}}$, and $F_{\text{width}}$ are the functions of non-uniform doping, channel length, and channel width dependencies, respectively.\(^7\) $K_{\text{etavb}}$ is the newly added parameter to represent reverse-to-forward $V_{\text{th}}$ dependencies to work with $K_{\text{eta}}$, which is a fitting parameter in BSIM4 model.

3. Experiment
The proposed model was implemented into SPICE3f5 and all the parameters were extracted from measured data. After the process instance parameters (physical dimensions and doping profiles) are defined, the model parameter extraction procedure consists of three simple steps. First, we extracted and optimized original BSIM4 DC parameters using a standard procedure which is written in BSIM4 manual\(^3\) or using any advanced commercial software such as MoDeCH Extractor.\(^15\) Secondly, $L_{\text{PD}}$ and $L_{\text{BS}}$ were optimized by using $V_{\text{th}}$ vs $V_{\text{BS}}$ measurement shown in Fig. 5. Finally, $K_{\text{eta}}$ and $K_{\text{etavb}}$ were optimized by using $I_{\text{DS}}$ vs $V_{\text{BS}}$ measurement shown in Fig. 8.

Figures 5 and 6 show $V_{\text{th}}$ vs $V_{\text{BS}}$ characteristic of measurement and simulations used by current BSIM4 and our modified BSIM4 models. It shows that the simulated $V_{\text{th}}$ by current BSIM4 has some differences under the forward bias condition, in contrast, our model agreed with the measured $V_{\text{th}}$ in sufficient accuracy. Since our threshold voltage equations include short channel effects, larger improvements of the forward $V_{\text{th}}$ dependencies are presented in Fig. 6.
Figure 7 shows $I_{DS}$ vs drain-to-source voltage ($V_{DS}$) with some $V_{GS}$ voltages under the reverse bias condition for measured and simulated current by BSIM4 and our proposed models. Both of simulated currents show equivalent accuracies. Figure 8 shows $I_{DS}$ vs $V_{DS}$ with some $V_{GS}$ voltages under the forward bias condition. The total rms error of the simulated current by proposed model agrees with measured data in sufficient accuracy which was about 3%, whereas the error with BSIM4 was about 50%. Thus we proposed the model and equations to implement in BSIM4 version 4.6 as an instance.

The proposed model improved the forward body biased drain current simulation accuracies without sacrificing simulation accuracies of the null and reverse biased drain current in 60 nm n-MOSFET process devices.

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6) BSIM [http://www-device.eecs.berkeley.edu/~bsim3].
7) BSIM4 [http://www-device.eecs.berkeley.edu/~bsim4].
8) HiSIM2: [http://home.hiroshima-u.ac.jp/usdl/HiSIM2/].
10) EKV3 [http://ekv.epfl.ch/].