

# A 0.7 V-to-1.0 V 10.1 dBm-to-13.2 dBm 60-GHz Power Amplifier Using Digitally-Assisted LDO Considering HCI Issues

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**Abstract**—A 60-GHz power amplifier (PA) with consideration of hot-carrier-induced (HCI) degradation is presented. The supply voltage of the last stage of the PA ( $V_{PA}$ ) is dynamically controlled by an on-chip digitally-assisted low drop-out voltage regulator (LDO) to alleviate HCI effects. The PA is fabricated in a standard 65-nm CMOS process with a core area of  $0.21 \text{ mm}^2$ , which provides a saturation power of 10.1 dBm to 13.2 dBm with a peak power-added efficiency (PAE) of 8.1% to 15.0% for  $V_{PA}$  varying from 0.7 V to 1.0 V at 60 GHz, respectively.

## I. INTRODUCTION

Wireless transceivers operating in the unlicensed 9-GHz band around 60 GHz in CMOS processes have been investigated and reported intensively in the past several years due to their capability of achieving low-cost multi-gigabit-per-second short-range wireless communications [1]–[3]. It is known that a power amplifier (PA) is one of the key blocks of wireless transceivers, the properties of which is crucial for the system performance, such as linearity, efficiency, communication distance, *etc.* For practical uses of 60-GHz CMOS PAs, reliability, suffering from hot carrier, bias temperature instability, time dependent dielectric breakdown and so on, is one of the most significant issues [4]. Particularly a thick-oxide transistor, a common solution for reliability issues at lower frequencies, can not be utilized for 60-GHz CMOS PA design because of its limited cut-off frequency ( $f_T$ ). Furthermore, as indicated in [5], hot-carrier-induced (HCI) effects are dominant for the reliability of the standard CMOS transistors in large-signal operation mode, which are generally used to realize the 60-GHz PAs.

Much effort has been carried out to solve the HCI issues for the 60-GHz CMOS PAs. Reducing the operation supply voltage [4] or using cascode topology [6] for the PAs can greatly alleviate the HCI effects on the PAs but at the cost of the degraded output power, linearity, and efficiency. A power combining technique [7] seems to be a promising solution for the HCI issues of the PAs while maintaining the superior performance. However, the deviation of the behavior of the power combiners at millimeter-wave frequencies from that of the lumped ones causes different phase delays for different paths of the PA deteriorating the modulation quality of the

transmitter and being sensitive to process variations.

In this paper, a 60-GHz digitally-assisted variable-supply-voltage PA is proposed and implemented to relieve the HCI influences on the circuit. A fully-integrated mixed analog-digital low drop-out voltage regulator (LDO) is designed to dynamically adjust the supply voltage of the last stage of the PA ( $V_{PA}$ ) between 0.7 V and 1.0 V. The adjustment of  $V_{PA}$  offers a possibility to meet different linearity, efficiency, output power and lifetime requirements for the PA in actual applications. The PA is capable of outputting 13.2 dBm saturation power ( $P_{sat}$ ), 10.2 dBm power at 1-dB compression point ( $P_{1dB}$ ) and achieving 15.0% peak power-added efficiency (PAE). The PA fabricated in a standard 65-nm CMOS process is insensitive to the process variation thanks to the tunable supply voltage.

## II. CIRCUIT ANALYSIS AND DESIGN

Fig. 1 shows the entire block diagram of the proposed 60-GHz digitally-assisted variable-supply-voltage CMOS PA. The whole system is composed of a mixed analog-digital LDO, a 3-stage differential PA and a digital control block with reference voltage generator. The mixed analog-digital LDO co-operating with the digital control block is used to dynamically tune the supply voltage  $V_{PA}$  for the last stage of the PA, which normally suffers the most from the HCI effects. The control scheme is briefly described as follows: when the transmitter does not require high output power and/or linearity,  $V_{PA}$  will be decreased to relieve the HCI stress. Otherwise  $V_{PA}$  will be maintained in a high level.

The LDO consists of a digital-tuning block, an analog-tuning block and an array of PMOSFETs, as can be seen in Fig. 1. The digital-tuning block [8], [9], including a dynamic comparator, an  $n$ -bit up/down counter and a digital/analog switching logic, is adopted and optimized in this work, because it consumes ultra-low power, can fully turn on the PMOSFETs achieving low voltage drop-out and easily accomplish fast recovery and tuning of the supply voltage  $V_{PA}$ . Where the fast recovery feature is necessary for multi-gigabit-per-second-throughput wireless transmitters operating in time division duplex mode (*e.g.* less than  $3 \mu\text{s}$  for over 2 Gb/s throughput) [2].

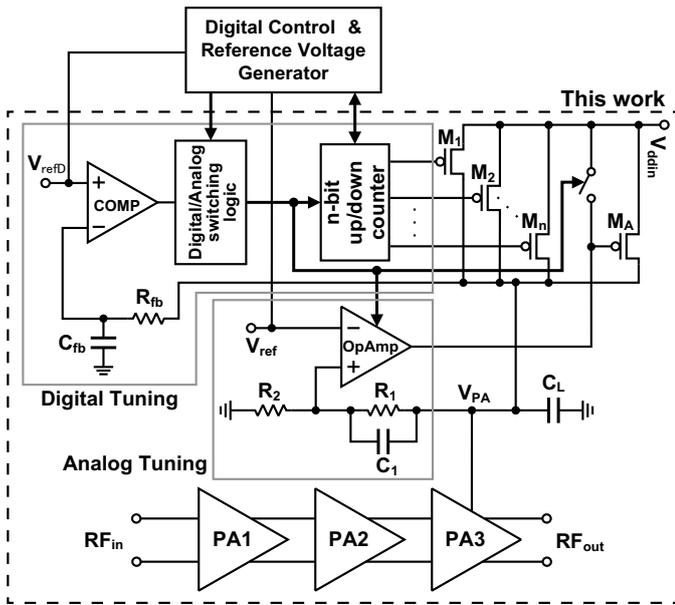


Fig. 1. System block diagram of the proposed 60-GHz digitally-assisted PA.

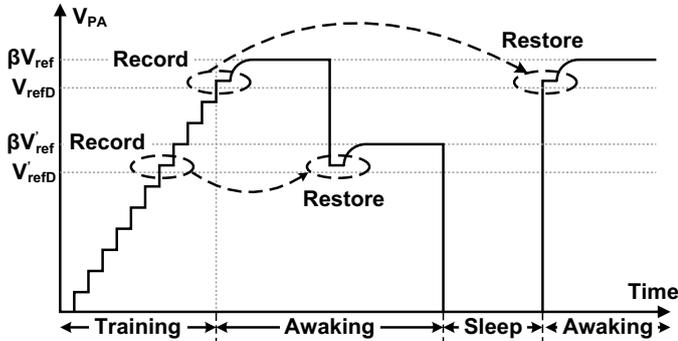


Fig. 2. The transient operation of the mixed analog-digital LDO.

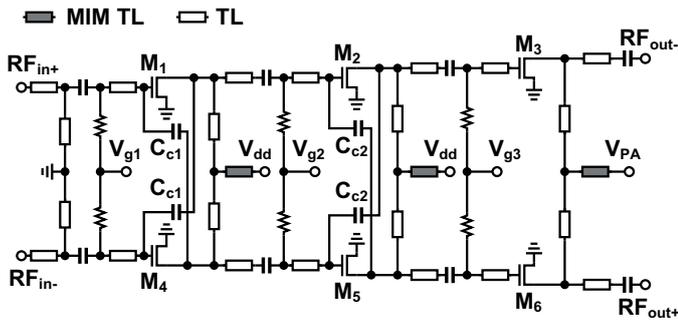


Fig. 3. The 3-stage differential PA core.

The analog-tuning block is utilized to avoid the inherently large ripple of the digital-tuning block when the 3-stage PA is working. Fig. 2 illustrates the transient operation of the mixed analog-digital LDO with the assistance of the digital control block for fast tuning and recovery of the supply voltage  $V_{PA}$ . At the beginning of the LDO operation, the digital-tuning block goes through a training period while analog-tuning block is turned off by the switching logic.  $V_{PA}$  is swept

from minimum to maximum value by adjusting the reference voltage of the digital-tuning block ( $V_{refD}$ ). The digital control bits of the PMOSFETs ( $M_1$  to  $M_n$ ) for different values of  $V_{refD}$  are recorded to the digital control block. Once the training period is finished, when the value of  $V_{PA}$  is larger than the setting value of  $V_{refD}$ , the LDO is switched from digital to analog mode by the switching logic. After a period of charging (or discharging), the LDO outputs a constant  $V_{PA}$  at the value of  $\beta V_{ref}$ , where  $\beta = (R_1 + R_2)/R_2$  and  $V_{ref}$  is the reference voltage of the analog-tuning block, as depicted in Fig. 2. When the desired value of  $V_{PA}$  is changed or/and the circuit is awakened from sleep mode, the digital control block restores the control bits for  $M_1$  to  $M_n$  to the up/down counter and generates reference voltages correspondingly.  $V_{PA}$  will be instantly charged (or discharged) to the value corresponding to the restored digital control bits, then tuned by the analog block of the LDO to the desired value in a short time. Simulation results show that the recovery time of  $V_{PA}$  is less than  $0.1 \mu s$ .

The schematic of the 3-stage differential CMOS PA is shown in Fig. 3. The HCI effects on the PA are further alleviated owing to the adoption of the differential topology. A transmission line (TL) with  $0.8 \text{ dB/mm}$  loss around  $60 \text{ GHz}$  is used for matching network, and an MIM transmission line (MIM TL) is realized for the de-coupling of the power supplies. The stability and power gain of the PA are improved by incorporating the capacitive cross-coupling technique for the first and second stages of the PA [10], [11].

### III. MEASUREMENT RESULTS

To verify our design, the core blocks of the proposed 60-GHz PA including the mixed analog-digital LDO and the 3-stage differential PA are fabricated in a standard  $65 \text{ nm}$  CMOS technology. Fig. 4 shows the die micro-photograph of the circuit. The areas of the 3-stage differential PA and the mixed analog-digital LDO are  $0.132 \text{ mm}^2$  and  $0.025 \text{ mm}^2$ , respectively. The on-chip de-coupling capacitor ( $C_L$ ) is  $86 \text{ pF}$  with a size of  $0.051 \text{ mm}^2$ . The supply voltage of the first and second stages of the PA ( $V_{dd}$ ) and the external input voltage of the LDO ( $V_{ddin}$ ) are set to be  $1.2 \text{ V}$  for demonstration simplicity.

As depicted in Fig. 5, the small-signal S-parameters of the PA is measured for different values of  $V_{PA}$ . The 3-dB bandwidth is about  $13 \text{ GHz}$  (from  $53 \text{ GHz}$  to  $66 \text{ GHz}$ ) for all the measurement values of  $V_{PA}$ . The peak gain is  $19.7 \text{ dB}$  and  $17.0 \text{ dB}$  at  $59 \text{ GHz}$  for  $V_{PA} = 1.0 \text{ V}$  and  $V_{PA} = 0.7 \text{ V}$ , respectively. The measured  $P_{sat}$ ,  $P_{1dB}$  and maximum PAE ( $PAE_{max}$ ) are plotted versus  $V_{PA}$  at  $60 \text{ GHz}$  in Fig. 6. The  $P_{1dB}$  is reduced from  $10.2 \text{ dBm}$  to  $5.8 \text{ dBm}$  when  $V_{PA}$  is tuned from  $1.0 \text{ V}$  to  $0.7 \text{ V}$  as can be observed in Fig. 6. The HCI stress on the circuit is therefore lightened by decreasing the supply voltage and output power simultaneously, which leads to a better lifetime for the proposed PA. In Fig. 7, the experimental lifetime of the NMOSFETs used in the last stage of the PA is illustrated under different stress conditions. The lifetime is defined as the time when the drain current

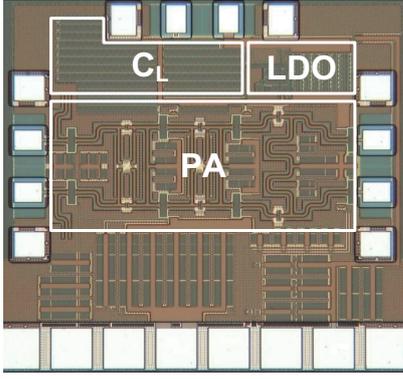


Fig. 4. Die micro-photograph. Chip size:  $0.70 \times 0.80 \text{ mm}^2$  including pads.

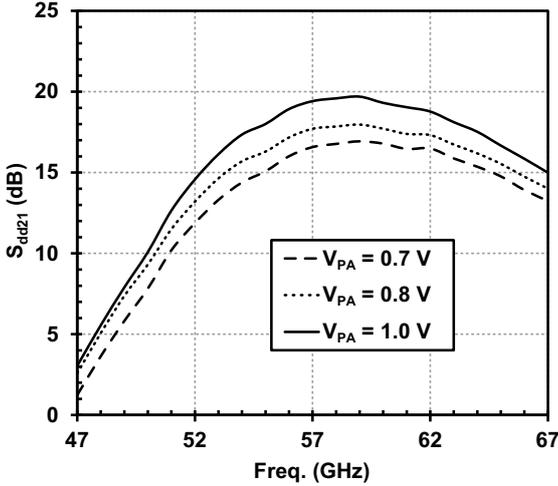


Fig. 5. Measured  $S_{dd21}$  for various values of  $V_{PA}$ .

of the transistor ( $I_{DS}$ ) decreases by 10% from the unstressed value. When the output power of the PA ( $P_{out}$ ) is 10 dBm and  $V_{PA} = 1.0 \text{ V}$ , the lifetime of the NMOSFETs is only 0.2 year. While if  $P_{out} = 5 \text{ dBm}$  and  $V_{PA} = 0.75 \text{ V}$ , the lifetime is improved to about 30 years.

Table I summarizes and compares the performance of the proposed power amplifier with that of the state-of-the-art PAs at 60 GHz in CMOS processes. It is shown in table I that the proposed PA exhibits comparable output power and efficiency at high supply voltage ( $V_{PA} = 1.0 \text{ V}$ ) to the recently published PAs in the 60-GHz band for CMOS technologies. Meanwhile, at low supply voltage ( $V_{PA} = 0.7 \text{ V}$ ), the proposed PA with reasonable output power, efficiency and linearity still can be used for shorter distance communications or/and low-level modulation schemes (e.g. BPSK and QPSK). As demonstrated in Fig. 8, the measured output spectrum of the proposed PA barely degrades when  $V_{PA}$  is reduced from 1.0 V to 0.7 V and output power is comparable. The measurement is performed by applying a QPSK modulation signal to the input of the PA at channel 3 (61.56 GHz to 63.72 GHz) of IEEE 802.15.3c with a symbol rate of 1.76 Gs/s. The center frequency of this channel is 62.64 GHz. Both of the spectrums meet the IEEE 802.15.3c standard. Fig. 9 shows the measured EVM

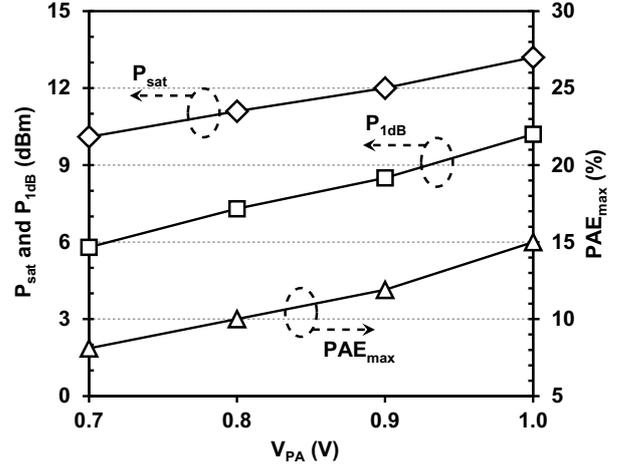


Fig. 6. Measured  $P_{sat}$ ,  $P_{1dB}$  and  $PAE_{max}$  versus  $V_{PA}$  at 60 GHz.

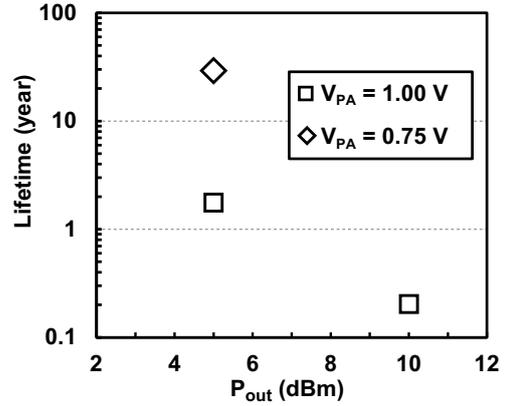


Fig. 7. Experimental lifetime of the NMOSFETs for different values of output power  $P_{out}$  and  $V_{PA}$ .

at various values of  $V_{PA}$  and  $P_{out}$ . The channel 3 of IEEE 802.15.3c and 3.52-Gb/s QPSK modulation signal are chosen again to evaluate the EVM performance of the proposed PA. All the measured EVM is lower than -17 dB and satisfies IEEE 802.15.3c standard. It can be observed that the measured EVM is from 11.7% (-18.6 dB) to 12.9% (-17.8 dB) for low output power ( $P_{out} = 5 \text{ dBm}$ ) if  $V_{PA}$  is tuned from 1.0 V to 0.7 V. The degradation of the EVM is less than 1 dB, which implies the low supply voltage  $V_{PA}$  is preferred for low output power situation considering the HCI issues. While at high output power ( $P_{out} = 10 \text{ dBm}$ ), the measurement value of the EVM is 13.1% (-17.7 dB) and 13.6% (-17.3 dB) for  $V_{PA} = 1.0 \text{ V}$  and  $V_{PA} = 0.9 \text{ V}$ , respectively.

#### IV. CONCLUSION

This paper presents a 60-GHz variable-supply-voltage power amplifier using the digitally-assisted LDO in a 65-nm CMOS process. The severe HCI issues for 60-GHz CMOS power amplifiers have been greatly alleviated at low supply voltage ( $V_{PA} = 0.7 \text{ V}$ ). The lifetime of the proposed PA can be improved to over 30 years. On the other hand, the power amplifier is still able to provide 13.2 dBm saturation power, 10.2 dBm power at 1-dB compression point and 15.0%

TABLE I  
60-GHz CMOS PA PERFORMANCE COMPARISON.

Ref.	CMOS Process	Freq. (GHz)	Supply (V)	$P_{\text{sat}}$ (dBm)	$P_{1\text{dB}}$ (dBm)	$\text{PAE}_{\text{max}}$ (%)	Area (mm <sup>2</sup> )
[4]	90 nm	60	0.7	8.5	5.2	7.0	0.18 (core)
			1.0	11.5	8.0	15.2	
[6]	65 nm SOI	60	1.2	10.5	7.1	22.3	0.573
			1.8	14.5	12.7	25.7	
			2.6	16.5	15.2	18.2	
[7]	65 nm	60	1.0	18.6	15.0	15.1	0.28
[11]	65 nm	60	1.0	11.5	8.0	15.2	0.696
This work	65 nm	60	0.7*	10.1	5.8	8.1	0.56
			1.0*	13.2	10.2	15.0	

\* Only for the last stage  $V_{\text{PA}}$

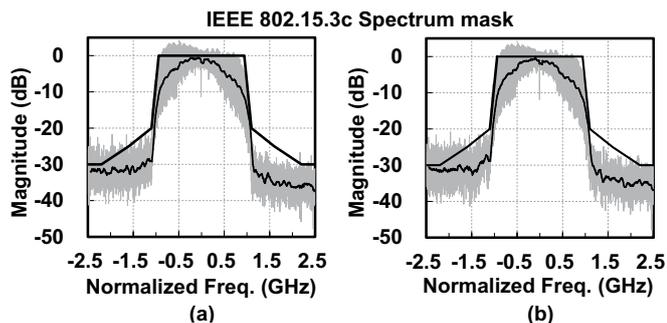


Fig. 8. Measured output spectrum of the proposed PA normalized to 62.64 GHz for QPSK modulation (a)  $V_{\text{PA}} = 1.0\text{ V}$ ,  $P_{\text{out}} = 4\text{ dBm}$ ; (b)  $V_{\text{PA}} = 0.7\text{ V}$ ,  $P_{\text{out}} = 3\text{ dBm}$ .

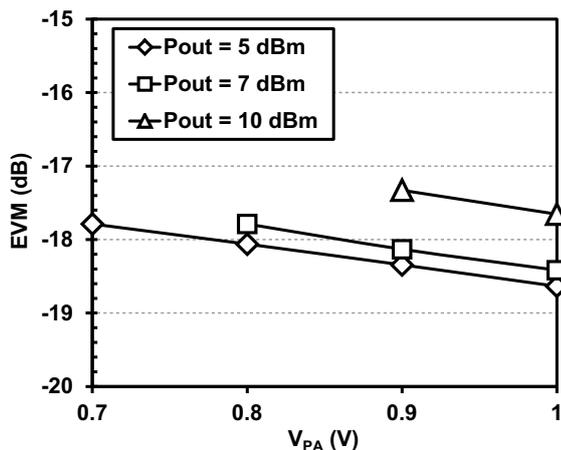


Fig. 9. Measured EVM versus  $V_{\text{PA}}$  for QPSK modulation at different output power level.

peak power-added efficiency at 60 GHz for high supply voltage ( $V_{\text{PA}} = 1.0\text{ V}$ ). The performance of the proposed PA at various  $V_{\text{PA}}$  conditions meets the requirements of short-range multi-gigabit-per-second communication standards (e.g. IEEE 802.15.3c).

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#### REFERENCES

- [1] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "A full 4-channel 6.3 Gb/s 60 GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 218–219.
- [2] T. Mitomo, Y. Tsutsumi, H. Hoshino, M. Hosoya, T. Wang, Y. Tsubouchi, R. Tachibana, A. Sai, Y. Kobayashi, D. Kurose, T. Ito, K. Ban, T. Tandai, and T. Tomizawa, "A 2 Gb/s-throughput CMOS transceiver chipset with in-package antenna for 60 GHz short-range wireless communication," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 266–267.
- [3] V. Vidojkovic, G. Mangraviti, K. Khalaf, V. Szortyka, K. Vaesen, W. V. Thillo, B. Parvais, M. Libois, S. Thijss, J. R. Long, C. Soens, and P. Wambacq, "A low-power 57-to-66 GHz transceiver in 40 nm LP CMOS with -17 dB EVM at 7 Gb/s," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 268–269.
- [4] M. Tanomura, Y. Hamada, S. Kishimoto, M. Ito, N. Orihashi, K. Maruhashi, and H. Shimawaki, "TX and RX front-ends for 60 GHz band in 90 nm standard bulk CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 558–559.
- [5] L. Negre, D. Roy, F. Cacho, P. Scheer, S. Jan, S. Boret, D. Gloria, and G. Ghibaudo, "Reliability characterization and modeling solution to predict aging of 40-nm MOSFET DC and RF performances induced by RF stress," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1075–1083, May 2012.
- [6] A. Siligaris, Y. Hamada, C. Mounet, C. Raynaud, B. Martineau, N. Deparis, N. Rolland, M. Fukaishi, and P. Vincent, "A 60 GHz power amplifier with 14.5 dBm saturation power and 25% peak PAE in CMOS 65 nm SOI," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1286–1294, Jul. 2010.
- [7] J. Chen and A. M. Niknejad, "A compact 1 V 18.6 dBm 60 GHz power amplifier in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2011, pp. 432–433.
- [8] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P.-H. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-mA quiescent current in 65 nm CMOS," in *Proc. IEEE CICC*, 2010, pp. 323–326.
- [9] K. Hirairi, Y. Okuma, H. Fuketa, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "13% power reduction in 16 b integer unit in 40 nm CMOS by adaptive power supply voltage control with parity-based error prediction and detection (PEPD) and fully integrated digital LDO," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 486–487.
- [10] H. Asada, K. Bunsen, K. Matsushita, R. Murakami, Q. Bu, A. Musa, T. Sato, T. Yamaguchi, R. Minami, T. Ito, K. Okada, and A. Matsuzawa, "A 60 GHz 16 Gb/s 16QAM low-power direct-conversion transceiver using capacitive cross-coupling neutralization in 65 nm CMOS," in *Proc. IEEE A-SSCC*, 2011, pp. 373–376.
- [11] W. L. Chan and J. R. Long, "A 58–65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, Mar. 2010.