Background and Motivation

This research is supposed to implement the most precise CMOS readout LSI in the world for 3D charged particle tracking applications by using standard deep sub-micro CMOS process.

**Functionality of pixel readout LSI**

- **Cathode**
- **Charged particle**
- **Induced current in pixel**
- **LSI (anode)**
- **Pixel PAD**

**Conventional TOT method**

- **Large resistor for constant discharge**
- **Semi-Gaussian shaper: differentiator and integrator**

- **Indirect measurement → not precise**
- **large discharge time ( > 500 ns ~ 1 μs) → Not suitable for fast imaging application**

**Requirements for new methods**

- **Total charge information is estimated from TOT**
- **But, TOT is affected by the flying angular**
- **To improve the charge detecting precision, new methods are necessary**

**Pixel Schematic of Qpix v.1**

**QPIX: Quad information / Quasi-3D / Q (Charge) information provided PIXel readout LSI**

**Dynamic comparator with capacitance calibration**

- Simulation results:
  - input offset voltage (σ): 13.5 mV → 1.5 mV
  - improves the detecting sensitivity

**SAR ADC**

- 10 bit, 10 Msp
- Low power consumption: no DC current
- Small die size: compact structure
Chip Implementation

**Measurement Results**

<table>
<thead>
<tr>
<th></th>
<th>Qpix v.1</th>
<th>Qpix v.0</th>
<th>Timepix</th>
<th>Future work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pixels</td>
<td>20 x 20</td>
<td>2 x 8</td>
<td>256 x 256</td>
<td>20 x 20</td>
</tr>
<tr>
<td>Pixel dimensions</td>
<td>200 x 200 μm² (Pixel pad included)</td>
<td>140 x 200 μm² (No pixel pad)</td>
<td>50 x 50 μm²</td>
<td>200 x 200 μm² (Pixel pad included)</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>10 fC ~ 1.5 pC</td>
<td>100 fC ~ 1.0 pC</td>
<td>0.1 fC ~ 12 fC</td>
<td>1 fC ~ 150 fC</td>
</tr>
<tr>
<td>Comp. threshold</td>
<td>35 fC</td>
<td>245 fC</td>
<td>0.1 fC</td>
<td>1 fC</td>
</tr>
<tr>
<td>Readout information</td>
<td>TOF: 14 bits, 10 ns</td>
<td>TOF: 14 bits, 10 ns</td>
<td>14 bits, 10 ns (TOF or TOT or Photon counter)</td>
<td>TOF: 14 bits, 10 ns</td>
</tr>
<tr>
<td></td>
<td>TOT: 8 bits, 10 ns</td>
<td>TOT: 8 bits, 10 ns</td>
<td>TOT: 8 bits, 10 ns</td>
<td>TOT: 8 bits, 10 ns</td>
</tr>
<tr>
<td></td>
<td>ADC: 10 bits, 10MSps</td>
<td>ADC: 6 bits, 10MSps</td>
<td>None</td>
<td>ADC: 10 bits, 10MSps</td>
</tr>
<tr>
<td>Power/channel</td>
<td>187.5 μW</td>
<td>350 μW</td>
<td>6.5 μW + 7 μW</td>
<td>150 μW</td>
</tr>
<tr>
<td>Readout speed</td>
<td>240 Mbps</td>
<td>100 Mbps</td>
<td>100Mbps</td>
<td>240 Mbps</td>
</tr>
<tr>
<td>Readout mode</td>
<td>Serial/Parallel</td>
<td>Switched parallel</td>
<td>Serial/Parallel</td>
<td>Serial/Parallel</td>
</tr>
</tbody>
</table>

*Offset charge is caused by large parasitic capacitance in measurement system.*

• 130 μm x 140 μm active circuitry
• large pixel pad
  – As an charge-collecting pad when used in gas chambers
  – As a bonding pad for flip-chip bump bonding with diverse sensors

• 0.18 μm CMOS process, 400 pixels
• Compact high speed readout structure: 240 Mbps
• Suitable for large area applications
  – 16 mm² active detection area (64% of the total chip surface)

(1) 10-bit SAR ADC; (2) TOT counter; (3) 10-bit register for ADC; (4) 5-bit calibration register for the amplifier; (5) TOF counter; (6) pixel control logic circuit; (7) 4-bit calibration register for comparator; (8) control signal buffers; (9) comparator; (10) the amplifier and the integrator; (11) pixel pad; (12) bonding point for flip-chip bump bonding.