An Improved Dual-Conduction Class-C VCO Using a Tail Resistor

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Contents

• Background
• Dual-Conduction Class-C VCO
• Simulation result
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• Conclusion
Scaling of supply voltage

Low voltage circuits are needed.

[1] ITRS 2009 ORTC
http://www.itrs.net/
Class-C VCO [2]

It realizes low phase noise

At low supply voltages, the oscillation is not robust.

Impulse Sensitivity Function \[ [3] \]

(a) No phase shifting

(b) Phase shifting

Operation of Class-C VCO

$V_{DD}$

$L$

$C_{tank}$

$V_{bias}$

$I_{bias}$

$C_{tail}$

$V_{gs}$

$V_{th}$

$V_{bias}$

ISF

Ideal current

Current waveform
Startup problem

At low supply voltage, the amplitude is very small.

The oscillation is not robust.
Dual-Conduction Class-C VCO\cite{4}

It works at 0.2 V supply voltage.

The pair for startup consumes power and degrades phase noise.

\cite{4} K. Okada, et al., VLSIC 2009
Add a resistor to the Source for startup

$V_s$ rise $\Rightarrow V_{gs}$, $V_{ds}$ fall

\[ I_{ds} \approx \frac{\mu C_{ox}}{2} (V_{gs} - V_{th})^2 \left( 1 + \frac{V_{ds}}{V_A} \right) \]

$I_{ds}$ for startup pair decrease

for Class-C

for startup
Simulation result

This work

with Resistor (10 Ohm)
without Resistor

$I_{DC} [\mu A]$ vs $V_{DD} [V]$
Simulation result

Phase Noise [dBc/Hz] @ 1MHz Offset

-102
-104
-106
-108
-110
-112
-114

0.2 0.3 0.4 0.5

$V_{DD}$ [V]

This work

with Resistor (10 Ohm)
without Resistor

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Simulation result

![Graph showing FoM vs. V_{DD}]

\[
\text{FoM} = \mathcal{L}(f_{\text{offset}}) - 20 \log \left( \frac{f_0}{f_{\text{offset}}} \right) + 10 \log \left( \frac{P_{DC}}{1 \text{ [mW]}} \right)
\]

10 October, 2011

Y. Takeuchi, Tokyo Tech
Amplitude shrink rate degrades phase noise and FoM

$\mathcal{L}(\Delta \omega) = 10 \log \left( \frac{2kT}{P_{\text{sig}}} \cdot \left( \frac{f_0}{2Q\Delta f} \right)^2 \right)$

Amplitude shrink rate [%] = \frac{At(0\Omega) - At(10\Omega)}{At(0\Omega)} \times 100
Chip micrograph

- CMOS 180 nm
- Core size 0.20 mm$^2$
- 10 Ohm tail resistor
Measurement result

\[ \begin{array}{|c|c|}
\hline
V_{DD} & 0.2 \text{ V} \\
\hline
\text{Frequency} & 5.4 \text{ GHz} \\
\hline
\text{Phase Noise} & -102 \text{ dBC/Hz} \quad @1\text{MHz Offset} \\
\hline
\text{Power} & 96 \mu \text{W} \\
\hline
\text{FoM} & -187 \text{ dBC/Hz} \\
\hline
\end{array} \]
## Performance summary

<table>
<thead>
<tr>
<th></th>
<th>[3]</th>
<th>[5]</th>
<th>[4]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS 0.13μm</td>
<td>CMOS 0.18μm</td>
<td>CMOS 0.18μm</td>
<td>CMOS 0.18μm</td>
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<tr>
<td>Supply voltage [V]</td>
<td>1.0</td>
<td>0.50</td>
<td>0.35</td>
<td>0.30</td>
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<td></td>
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<td>0.20</td>
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<td>DC Power [μW]</td>
<td>1300</td>
<td>570</td>
<td>1460</td>
<td>630</td>
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<td>114</td>
<td>96</td>
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<tr>
<td>Frequency [GHz]</td>
<td>4.9</td>
<td>3.8</td>
<td>1.4</td>
<td>5.4</td>
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<tr>
<td>Phase noise [dBc/Hz]</td>
<td>-130 @3MHz</td>
<td>-119 @1MHz</td>
<td>-129 @1MHz</td>
<td>-113 @1MHz</td>
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<tr>
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<tr>
<td>FoM [dBc/Hz]</td>
<td>-196</td>
<td>-193</td>
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<tr>
<td>Topology</td>
<td>Class-C (single)</td>
<td>Transformer feedback</td>
<td>Dual-Conduction Class-C</td>
<td>Dual-Conduction Class-C</td>
</tr>
</tbody>
</table>

Conclusion

• We added a resistor to the source of transistors for startup of Dual-Conduction Class-C VCO.

• In the simulation, it reduced power consumption and improved phase noise in more than 0.35 V supply voltage.

• We fabricated the proposed VCO. It operates at 0.2V supply voltage and consumes only 96 $\mu$W.
Thank you for your attention