An Improved Dual-Conduction Class-C VCO Using a Tail Resistor

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Abstract—This paper proposes a method to improve the power consumption of dual-conduction class-C VCO. The dual-conduction class-C VCO has two pairs of cross-coupled transistors for low supply voltage operation. One is a main pair for the class-C operation, the other is an auxiliary pair for startup. The auxiliary pair continues to operate after the VCO starts class-C operation, which consumes additional power. Thus, we added a resistor to the source node of the auxiliary pair. Since the resistor reduces the current of the auxiliary pair, the power consumption can be improved. The proposed VCO is fabricated by using a 0.18\(\mu\)m CMOS technology. It oscillates at 5.4 GHz with 0.20 V supply voltage, consumes 96\(\mu\)W, and achieves a FoM of -187 dBc/Hz.

I. INTRODUCTION

High-speed digital circuits require low power, low noise clock generation. The scaling of CMOS technology has decreased the supply voltage and the power consumption. However, at lower supply voltages, since the amplitude is small, the phase noise is degraded due to the small signal power. It is difficult to cope with both low power and low phase noise.

The class-C VCO has been proposed for low phase noise operation [1], [2]. It has an independent gate bias and a tail capacitor. The gate bias is set lower than the threshold voltage. Whereas, the tail capacitor makes the current waveform sharp. Due to the lower gate bias and the impulse-shape current waveform, the phase noise is low. However, because of the lower gate bias, it cannot oscillate at low supply voltages.

The dual-conduction class-C VCO has been proposed at ultra-low supply voltage [3]. It has two pairs of cross-coupled transistors. One is a main pair for class-C operation, the other is an auxiliary pair for startup. The gate bias of the auxiliary pair is higher than that of the main pair. Due to the higher gate bias, it can oscillate at ultra-low supply voltages such as 0.20 V. However, the auxiliary pair degrades the FoM after the VCO starts class-C operation. It consumes additional power, and the higher gate bias degrades the phase noise.

In the proposed topology, a resistor is added to the source node of the auxiliary pair. This simple method does not require additional circuits and power dissipation. Since the resistor increases the source voltage, the transistors current is reduced at the stable state. Hence, the power consumption can be improved.

II. CLASS-C VCO

This section describes the impulse sensitivity function (ISF) [4], [5] at first, and then describes the operation of class-C VCOs using the ISF.

A. Impulse Sensitivity Function (ISF)

The impulse sensitivity function (ISF) shows the sensitivity to the phase noise of oscillators. In case of Fig. 1(a), the noise is injected at the peak of the voltage waveform, and it increases the amplitude. However, the waveform will return to its original amplitude because of the stability of oscillation amplitude as shown in Fig. 1(a). On the other hand, in case of Fig. 1(b), the noise injection also causes increase the voltage. However, the voltage increase causes a phase shift and it cannot be recovered even though the amplitude is stable. Thus, the noise sensitivity of Fig. 1(b) is higher than that of Fig. 1(a).

As mentioned above, the sensitivity depends on the phase of the voltage waveform. The ISF becomes zero at the peaks of the voltage waveform, and takes a maximum value at zero-crossing points.

B. Class-C VCO

According to the discussion in the above section, the current of oscillators should be conducted at the timings when the ISF
becomes zero, and the class-C VCO realizes such the ideal current conduction [1], [2].

The class-C VCO has two features. One is the tail capacitor \((C_{\text{tail}})\), which makes the current waveform sharp. The other is the independent gate bias \((V_{\text{bias}})\), and it is set lower than the threshold voltage. Fig. 2 shows the current waveform. The black line shows the waveform of the left transistor, and the gray line shows that of the right transistor. Since the gate bias \((V_{\text{bias}})\) is set lower than the threshold voltage \((V_{\text{th}})\), the conduction time becomes shorter than the half period. The shorter conduction time and the impulse-shape current waveform improve the phase noise, thanks to their effective ISF.

To improve the phase noise, the gate bias should be set as low as possible. However, the lower gate bias causes the startup problem. To turn on a transistor, the amplitude has to satisfy Eq. (1).

\[
V_{\text{bias}} + A_t > V_{\text{th}} \\
A_t > V_{\text{th}} - V_{\text{bias}}
\]

where \(V_{\text{bias}}\) is the gate bias of the transistor, \(V_{\text{th}}\) is the threshold voltage, and \(A_t\) is the amplitude. At the startup state, since \(A_t\) is very small, it is difficult to obtain the transconductance with lower \(V_{\text{bias}}\). Actually, the oscillators can start oscillating by the sub-threshold current of CMOS transistors. However, it is not so robust. On the other hand, lower \(V_{\text{bias}}\) is required to improve the phase noise performance. Thus, there is a trade-off between the phase noise and the startup robustness. This is called the startup problem.

III. DUAL-CONDUCTION CLASS-C VCO

A. Dual-conduction class-C VCO

The conventional single-conduction class-C VCO has the startup problem, and it cannot perform well with low supply voltages. To solve the problem, the authors have proposed the dual-conduction class-C VCO [3]. It has two pairs of cross-coupled transistors. One is a main pair for class-C operation, the other is an auxiliary pair for the startup. The gate bias of the auxiliary pair is higher than that of the main pair. Thanks to the auxiliary pair, this VCO can start oscillating at the ultra-low supply voltage such as 0.20 V [3]. Furthermore, the gate bias of the main pair can be set much lower than the single-conduction class-C VCO. Hence, the dual-conduction class-C VCO can operate with low phase noise at ultra-low supply voltages.

However, the auxiliary pair degrades the FoM for two reasons. One reason is the problem of increased power consumption. The auxiliary pair even continues to operate after the VCO starts the class-C operation. Thus, it consumes additional power. The other reason is the problem of the phase noise. Owing to the higher gate bias, the conduction time becomes longer. The longer conduction time degrades the phase noise.

B. The proposed circuit

As mentioned above, the auxiliary pair degrades the FoM. Hence, the auxiliary pair should be suppressed after the VCO enters a steady oscillation state.

Eq. (2) gives the current of the transistor in the saturation region.

\[
I_{\text{ds}} = \frac{\mu C_{\text{ox}}}{2} \frac{W}{L} (V_{\text{gs}} - V_{\text{th}})^2 (1 + \lambda V_{\text{ds}})
\]

where \(I_{\text{ds}}\) is the current of the transistor, \(\mu\) is the charge-carrier effective mobility, \(C_{\text{ox}}\) is the gate oxide capacitance...
per unit area, \( W \) is the gate width, \( L \) is the gate length, \( V_{gs} \) is the gate-source voltage, \( V_{th} \) is the threshold voltage, \( \lambda \) is the channel-length modulation parameter, and the \( V_{ds} \) is the drain-source voltage. According to Eq. (2), \( V_{gs} \) and \( V_{ds} \) should be reduced to suppress the auxiliary pair current. In other words, the source voltage should be increased to reduce the pair current. To increase the source voltage, a resistor is added to the source node as shown in Fig. 3. Once the VCO starts oscillating, the current becomes larger. Since the source voltage becomes higher due to the resistance, \( V_{gs} \) and \( V_{ds} \) are reduced. Hence, the current of the auxiliary pair reduces as shown in Fig. 4.

C. Simulation results

Figs. 5 and 6 show the simulation results of a 10Ω resistor added to the dual-conduction class-C VCO using 0.18\( \mu \)m CMOS parameters. Fig. 5 shows a comparison between the conventional and proposed dual-conduction class-C VCOs. The FoM is calculated by Eq. (3) [6], which can be improved with more than 0.35V supply voltage,

\[
\text{FoM} = \mathcal{L}(f_{\text{offset}}) - 20 \log_{10} \left( \frac{f_0}{f_{\text{offset}}} \right) + 10 \log_{10} \left( \frac{P_{DC}}{1[\text{mW}]} \right) \tag{3}
\]

where \( \mathcal{L}(f_{\text{offset}}) \) is the phase noise, \( f_{\text{offset}} \) is the offset frequency, \( f_0 \) is the oscillation frequency, and \( P_{DC} \) is the power consumption. To determine why the FoM do not improve below 0.35V supply voltage, the amplitude change is investigated. Fig. 6 shows the amplitude shrink rate calculated by Eq. (4).

\[
(\text{Amplitude shrink rate})[\%] = \frac{A_{\text{t}(0\Omega)} - A_{\text{t}(10\Omega)}}{A_{\text{t}(0\Omega)}} \times 100 \tag{4}
\]

where \( A_{\text{t}(0\Omega)} \) is the amplitude without the resistor, and \( A_{\text{t}(10\Omega)} \) is the amplitude with 10Ω resistor. Since the phase noise is calculated by Eq. (5) [4], reduction of the amplitude degrades the phase noise and the FoM,

\[
\mathcal{L}(\Delta\omega) = 10 \cdot \log_{10} \left( \frac{FkT}{P_{\text{sig}}} \left( \frac{\omega_0}{2Q\Delta\omega} \right)^2 \right) \tag{5}
\]

where \( \Delta\omega \) is the offset frequency, \( F \) is the noise factor, \( k \) is Boltzmann constant, \( T \) is the absolute temperature, \( P_{\text{sig}} \) is the signal power, \( \omega_0 \) is the oscillation frequency, and \( Q \) is the Q-factor of the oscillator.

Since excessive reduction of the amplitude degrades the phase noise as shown in Figs. 5 and 6, the resistance should be carefully optimized.

IV. MEASUREMENT RESULTS

The proposed VCO is fabricated by using a 0.18\( \mu \)m CMOS technology. Fig. 7 shows the chip micrograph, and the core area is 0.18\( \text{mm}^2 \). The VCO can oscillate at 5.4 GHz with 0.2V supply voltage. The power consumption is 96\( \mu \)W. The phase noise is -102 dBc/Hz at 1 MHz offset, and the FoM is -187 dBc/Hz. Fig. 8 shows the measurement result of the phase noise, and Fig. 9 shows the measurement result of the FoM. In Fig. 5 (simulation), the FoM takes minimum value at 0.35V. However, in Fig. 9 (measurement), it becomes around
TABLE I
性能概要

<table>
<thead>
<tr>
<th>Technology</th>
<th>[1]</th>
<th>[7]</th>
<th>[3]</th>
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<td>CMOS</td>
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<td>-109</td>
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<tr>
<td>FoM([dBc/Hz])</td>
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<td>Transformer feedback</td>
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Fig. 8. 测量结果的相位噪声。

Fig. 9. FoM 测量结果。

0.50 V。这是由于尾电阻上的串联寄生电阻造成的。它减少了电流，从而降低了相位噪声和 FoM。因此，信号功率降低，然后相位噪声和 FoM 小于 0.50 V。

表 1 总结了 LC-VCOs 的状态-性能结果。提出的电路可以在低电压条件下实现非常低的功率消耗和优异的相位噪声性能。

V. CONCLUSION

在这个论文中，我们提出了一种新的双导通类-C VCO，它具有一个额外的尾电阻以减少功率消耗的辅助电对的稳态振荡状态。提出的电路可以在低电压条件下成功地工作，并且可以在 5.4 GHz 处以 FoM 为 -187 dBc/Hz 振荡。它仅消耗 96 \(\mu W\) 的功率，当电压为 0.20 V 时。因此，提出的类-C VCO 实现了超低功率操作与出色的相位噪声性能。

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