An Analysis on a Pseudo-Differential Dynamic Comparator with Load Capacitance Calibration

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An Analyzed Comparator

- CLK\textsubscript{Latch} becomes high
  1. Electric charge on the node Out\textsubscript{int} flows into gnd
  2. Current difference is determined by input signals
    - The difference is integrated on Out\textsubscript{int} and becomes larger as time passes
  3. The second stage regenerates the voltage difference

Fig. Transient waveform of a comparator [6], [7].


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D. Paik, Tokyo Tech.
Analysis Conditions of a Pre-amplifier

- Process is 90-nm CMOS
- The size of all transistors is 2 µm/100 nm
- To simplify the analysis
  - The rising time of \( \text{CLK}_{\text{Latch}} \) to 1 ps
  - \( M_3 \) and \( M_4 \) are in the deep triode when \( \text{CLK}_{\text{Latch}} \) is high
    - \( V_{\text{out\_int}} \) can be approximated as the drain voltage of \( M_1 \) (or \( M_2 \))

\[
V_{\text{out\_int}} = V_{dd} - \frac{I_{DS}}{C} \cdot t
\]

Fig. Simplified schematic of a dynamic amplifier when the \( \text{CLK}_{\text{Latch}} \) is high.
Mismatch Contribution

- Mismatch is dominated by a pair of input transistors
  - Mismatch of the second stage is suppressed by the gain of the pre-amplifier
  - $I_{DS}$ is mainly decided by input transistors
    - Mismatch changes $I_{DS}$ and the slew rate of $Out_{int}$ is also varied

$$V_{out_{int}} = V_{dd} - \frac{I_{DS}}{C} t \quad \Rightarrow \quad \frac{dV_{out_{int}}}{dt} = -\frac{I_{DS}}{C}$$

- Load capacitance calibration [2], [3] is commonly used to compensate mismatch
  - To figure out the calibration effect, the gain is required

Fig. Mismatch contribution (Remains are 2.4 %).

Channel-Length Modulation

• $I_{DS}$ is affected by the channel-length modulation
  – $\lambda$ is the channel-length coefficient

\[
I_{DS} = \frac{1}{2} \mu C_{OX} \frac{W}{L} V_{eff}^2 \left( 1 + \lambda \left( V_{DS} - V_{DS_{sat}} \right) \right)
\]

$V_{out\_int} = V_{dd} - \frac{I_{DS}}{C} t$

Fig. Influence of the channel-length modulation.

- $V_{eff} = V_{GS} - V_{th}$
- $V_{DS_{sat}} = \text{the saturation condition of drain-source voltage} = V_{eff}$
Gain of A Dynamic Amplifier

- $G_{\text{amp\_trans}}$ is satisfied only when $V_{\text{out\_int}} \geq V_{\text{eff}}$
  - If $V_{\text{out\_int}}$ falls to $V_{\text{eff}}$, $G_{\text{amp\_trans}}$ reaches its maximum

\[
G_{\text{amp\_trans}} = \frac{v_{\text{out}}}{v_{\text{in}}} = -\frac{i_{\text{DS}}}{C} \times \frac{1}{v_{\text{in}}} = \frac{2(V_{\text{dd}} - V_{\text{DS}})}{V_{\text{eff}}} \times \frac{1 + \frac{\lambda}{2}(V_{\text{DS}} - V_{\text{eff}})}{V_{\text{eff}}}
\]

**Fig.** Gain of a pre-amplifier.
Load Capacitance Calibration

- Using binary-weighted PMOS varactors
- By turning on or off PMOS, capacitance is varied
  - Reduce offset voltage

**Fig.** Load capacitance calibration.

**Capacitors for calibration**
(A number of unit cap. at each code = \(2^D\))

**Fig.** Error reduction by calibration
\(V_{\text{inp}} = V_{\text{inn}}\).
Input-Referred Compensated Voltage

• **Assumption**
  – Input signal of the second stage is decided when gain reaches its maximum

\[
v_{in\text{-diff_cal}} = \left( \frac{dV_{out\text{-int}}}{dC} \right)_{\text{input-referred}} \times \Delta C_{\text{cal}}
\]

\[
= -\frac{V_{\text{eff}}}{C} \times \left( 1 + \frac{1}{2} \left( V_{\text{dd}} - V_{\text{eff}} \right) \right) \times \left( N_{\text{Code}} - 2^{N_{\text{Cal}} - 1} \right) \times (C_{\text{on}} - C_{\text{off}})
\]

• \((N_{\text{Code}} - 2^{N_{\text{Cal}} - 1})\): \(\Delta N_{\text{Code}}\) from the middle of calibration code
  
  \(N_{\text{Code}}\): calibration code
  
  \(N_{\text{Cal}}\): calibration resolution

• \((C_{\text{on}} - C_{\text{off}})\): **capacitance difference** of a unit PMOS varactor
  
  \(C_{\text{on}}\): on capacitance of a unit PMOS varactor
  
  \(C_{\text{off}}\): off capacitance of a unit PMOS varactor
Simulation Results

- Simulation condition
  - 1 LSB = 1.5 mV
  - $V_{dd} = 1.0$ V and $V_{in\_com} = 0.5$ V
  - Size of a unit varactor is $W/L = 600 \text{ nm}/100 \text{ nm}$

\[
\text{Estimation: } \frac{V_{\text{eff}}}{C} \times \left(1 + \frac{\lambda}{2} (V_{dd} - V_{\text{eff}})\right) \times \left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right) \times (C_{on} - C_{off})
\]

![Graph showing input-referred compensated voltage by the capacitance calibration.](image)

**Fig.** Input-referred compensated voltage by the capacitance calibration.
PVT Variation

- If surrounding condition is varied after compensation, **calibration accuracy is degraded**
  - Process is fixed in the factory
  - **Voltage** and **Temperature** should be considered

- **Assumption**
  - An error due to PVT variation, $\sigma_{V_{PVT}}$, is **uncorrelated** with offset after calibration, $\sigma_{V_{offset}}$

\[
\sigma^2_{V_{offset}} = \sigma^2_{V_{offset0}} + \sigma^2_{V_{PVT}}
\]

($\sigma_{V_{offset0}}$ is extracted from simulation data)
Input Common-Mode Voltage

- Input common-mode voltage is fluctuated
- Standard deviation of calibration code is $\sigma_{\text{Code}}$

Error due to $V_{\text{eff}}$

$$\frac{\partial V_{\text{in\_diff\_cal}}}{\partial V_{\text{in\_com}}} \times \Delta V_{\text{in\_com}}$$

$$\Delta V_{\text{eff}} \left(1 + \frac{\lambda}{2} \left(V_{\text{dd}} - V_{\text{eff}}\right)\right) \times (C_{\text{on}} - C_{\text{off}}) \sigma_{\text{Code}}$$

Error due to $\lambda = \frac{V_{\text{eff}}}{C} \times (V_{\text{dd}} - V_{\text{eff}}) \frac{\Delta \lambda}{2} \times (C_{\text{on}} - C_{\text{off}}) \sigma_{\text{Code}}$

Error due to $(V_{\text{dd}} - V_{\text{eff}}) = -\frac{V_{\text{eff}}}{C} \times \frac{\lambda}{2} \Delta V_{\text{eff}} \times (C_{\text{on}} - C_{\text{off}}) \sigma_{\text{Code}}$

$$\sigma_{V_{\text{PVT\_VCOM}}} = \frac{V_{\text{eff}}}{C} \left(1 + \frac{\lambda}{2} \left(V_{\text{dd}} - V_{\text{eff}}\right)\right)$$

$$\times \sqrt{\left(\frac{\Delta V_{\text{eff}}}{V_{\text{eff}}} - \frac{\lambda \Delta V_{\text{eff}}}{V_{\text{eff}} - 2 + \lambda (V_{\text{dd}} - V_{\text{eff}})}\right)^2 + \left(\frac{(V_{\text{dd}} - V_{\text{eff}}) \Delta \lambda}{2 + \lambda (V_{\text{dd}} - V_{\text{eff}})}\right)^2} \times (C_{\text{on}} - C_{\text{off}}) \sigma_{\text{Code}}$$
Simulation Results

- Calibration is conducted when $V_{dd}$ is 1.0 V, $V_{in\_com}$ is 0.5 V, and Temp is 27 °C

\[
\begin{align*}
\text{SNDR decrease} & = \text{SNDR} - \text{SQNR} \\
& = -10 \log \left( 1 + \frac{12}{V^2} \sigma_v^2 \right)
\end{align*}
\]

![Graph](image)

**Fig.** Influence of input common-mode voltage on the capacitance calibration (1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).
Influence of Supply Voltage

- Calibration is conducted when $V_{dd}$ is 1.0 V, $V_{in\_com}$ is 0.5 V, and Temp is 27 °C.

$$\sigma_{V\_PVT\_Vdd} = \frac{V_{eff}}{C} \times \left(1 + \frac{\lambda}{2} \left(V_{dd} - V_{eff}\right)\right)$$

$$\times \left(\frac{\lambda \Delta V_{dd}}{2 + \lambda \left(V_{dd} - V_{eff}\right)}\right)$$

$$\times \left(C_{on} - C_{off}\right) \sigma_{Code}$$

Fig. Influence of supply voltage on the capacitance calibration
(1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).
Influence of Temperature

• Calibration is conducted when $V_{dd}$ is 1.0 V, $V_{in\_com}$ is 0.5 V, and Temp is 27 °C

**Fig.** Influence of temperature on the capacitance calibration (1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).
Conclusions

• A pseudo-differential dynamic comparator with load capacitance calibration is analyzed
  – The gain of a dynamic amplifier
    • Expressed by a ratio of $V_{dd}$ to $V_{eff}$ and $\lambda$ of an input transistor
    • Gain is inversely proportional to $V_{eff}$
  – Thermal noise, input-referred compensate voltage, and influence of PVT variation are analyzed
    • A dynamic comparator is sensitive to PVT variation
      – Mainly decided by $V_{eff}$
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References