

Two-Stage Band-Selectable CMOS Power Amplifier

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A power amplifier (PA), one of the key building blocks in RF transceivers, amplifies a signal at transmitter, so that the signal can reach farther. To transmit the signal far away, the conventional PA is implemented by compound semiconductor capable to use higher supply voltage related to a large output power. Therefore, the PA used to be realized as a discrete component. However, the PA is desired to be integrated in a single-chip transceiver which integrates all functional blocks for wireless communications in the view of cost, die occupancy, and so on. Thus, the PA is preferable to be implemented by CMOS process. The miniaturization of the recent CMOS transistors can provide a sufficient ability for PA and realize high frequency operation for RF circuits.

Moreover, there are various wireless communication standards which are using different frequency. Thus, Software Defined Radio Technology (SDR) is required. The software defined radio is a technology to realize various communication standards by only one transceiver, which can be updated by software. To realize the SDR system, a multi-standard RF front-end including a multi-band PA is required.

Fig. 1 shows the proposed power amplifier. The PA consists of two-stage and is utilizing a transformer at output end to obtain a large output power with high efficiency. Moreover, the frequency is selected by switching of inter-stage impedance.

If an impedance is not adjusted a complex conjugate between the first-stage and the second-stage, the output power from the first-stage is not fully transferred to the second stage. Therefore, an inter-stage to match the impedance between the output of the first stage and the input of the second stage is necessary. To realize a broadband stage-to-stage matching in minimum loss, circuit like Fig. 2 is proposed. A cascode topology is used in the first stage and the second stage. Common-gate transistors of the first stage and common-source transistors of the second stage are prepared for each band. The bias voltage and the electric current flows only on the transistor of selected band. In the case of figure, L-shaped matching which consists of L_I and C_I is effective. As the result, switching with an inductor and a capacitance is realized.

Moreover, the proposed PA employed a transformer at output end to obtain high output power and high power added efficiency (PAE). The saturated output power and the output impedance are an inverse relationship. Thus, the PA can achieve a higher output power with high PAE by an impedance conversion of a transformer.

Besides, capacitive cross-coupling used at the second stage is utilized to reduce a die area of the bypass capacitance. Though the area for inductor and transformer is dominant, the decrease of bypass capacitance is desirable. Additionally, the reduction of feedback capacitance improves reverse isolation.

Fig. 3 shows the chip micrograph. The chip was fabricated by 0.18 μm CMOS process using thick gate-oxide transistors and MIM capacitors. The total size is $1.18 \times 1.60 \text{ mm}^2$. The measurement results are given by Fig. 4 and Fig. 5. Fig. 4 shows the small signal S-parameters of the PA. The solid line shows simulation results, and the dotted line shows measurement results. Compared to the simulation results, a decreased gain and a shifted frequency are seen in some bands. The source of the error is thought to be due to a gap between real characteristic and electromagnetic field simulation result of transformer, a parasitic inductance which is not extracted of wiring, and an influence of the extraction accuracy of the parasitic components, *etc.* However, there is still a good correlation between the simulation and measurement results. Fig. 5 shows the saturated output power, the output 1-dB compression point, and the peak point of power added efficiency (PAE_{peak}) versus frequency. The saturated output power is larger than 25 dBm, and the output 1-dB compression point is larger than 21 dBm, and the PAE_{peak} is larger than 15 % over all frequency range. Table 1 summarizes the performance of the PA in this paper and shows the comparison with other wideband CMOS PAs.

In this paper, band-selectable power amplifier was proposed. The PA demonstrates that it has advantages like a band-selectable ability within a desired frequency range and a realization of CMOS PA with high power efficiency.

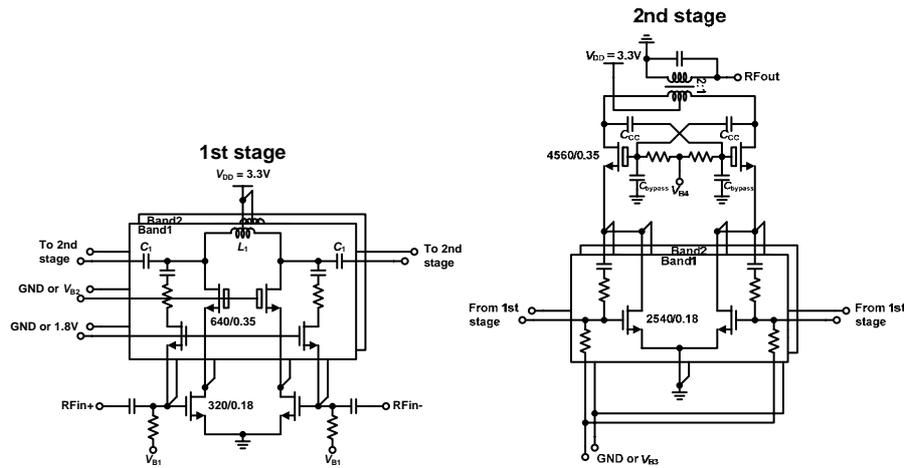


Figure 1. Schematic of the proposed power amplifier.

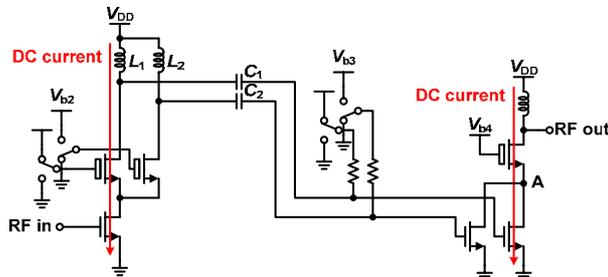


Figure 2. Changeover of inter-stage matching.

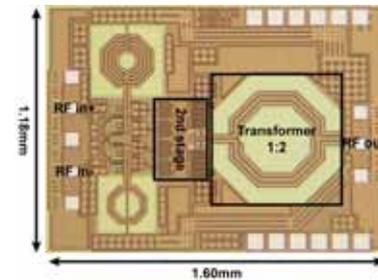


Figure 3. Chip micrograph.

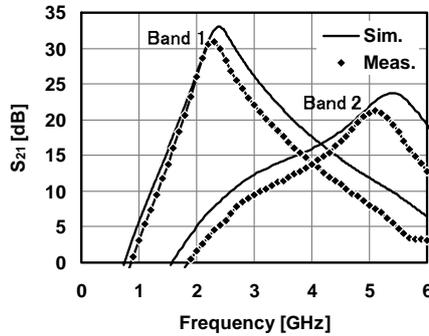


Figure 4. Measured S_{21} .

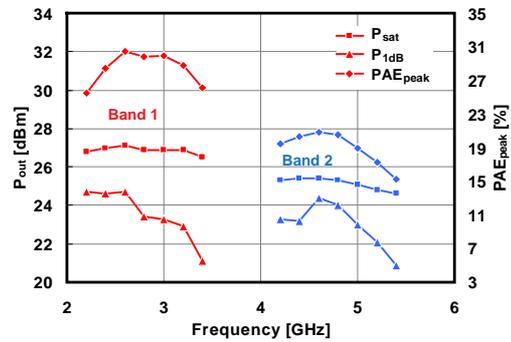


Figure 5. Measured P_{sat} , P_{1dB} , PAE_{peak} vs. frequency

Table 1. Performance comparison of CMOS PAs.

	Technology	V_{DD}	Frequency [GHz]	P_{sat} [dBm]	P_{1dB} [dBm]	PAE_{peak} [%]	Area [mm ²]
[1]	0.13 μ m CMOS	1.5 V	0.5 ~ 5.0	14 ~ 21	10 ~ 17	3 ~ 16	3.6
[2]	0.13 μ m CMOS	1.5 V	2.4 / 3.5	19	-	43	1.3
[3]	0.18 μ m CMOS	3.3 V	2.1 ~ 6.0	18 ~ 22	15 ~ 18	9 ~ 17	0.97
This work	0.18 μ m CMOS	3.3 V	2.2~3.4, 4.2~5.4	25 ~ 27	21 ~ 25	15 ~ 30	1.89

DE: Drain Efficiency

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