Motivation

- 6~7 bit, around 1 GS/s ADCs have many applications
  - Disk drive front-ends, ultra-wideband receivers
- Low power operation is most important issue for portable applications and green IT regulation

Problem of conventional topology

- Static power consumption in resistor ladder
- Large resistance causes settling problem
  - There is a trade-off between power consumption and settling time

Proposed ADC Architecture

- 4 b coarse stage and 3 b fine stage
  - Fine stage is interleaved to relax settling time
- CDAC with a S&H circuit achieves low power consumption and fast settling time
  - For 700 MS/s operation, RDAC consumes 1.8 mW but CDAC is only 0.38 mW

Gate-weighted Interpolation

- Double-tail latched comparator is introduced for lower input noise
  - Capacitive calibration reduces offset to 0.9 mV at 1
- Interpolation scheme reduces S&H circuits

Measurement Results

- DNL and INL are less than +0.6/-0.6 and +0.8/-0.6, respectively
- SNDR keeps 34 dB until Nyquist at 700 MS/s

ADC Performance Table (6 bit)

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<td>34/30</td>
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<td>32</td>
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<td>0.13</td>
<td>1.2</td>
<td>Subrange</td>
</tr>
</tbody>
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Block diagram of the conventional subranging ADC

Interpolation scheme reduces S&H circuits

Measurement Results

SNDR keeps 34 dB until Nyquist at 700 MS/s

ADC Performance Table (6 bit)