A 6-10 GHz Tunable Power Amplifier for Reconfigurable RF Transceivers

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Contents

- Introduction
- PA design
- Measurement results
- Conclusion
Introduction

- **PA (Power Amplifier):** A circuit used to convert a low-power RF signal into a larger signal of significant power at the transmitter.

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Introduction

- Single chip transceiver is demanded because of its low cost and downsizing.

Matsuzawa & Okada Lab.

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Various wireless communication standards

- ~ 6GHz : Various applications
- 6~10GHz : Potential application
Conventional wideband PA

- Distributed power amplifier

- Wideband input / output matching
  - Possibility of intermodulation

- Lack of the optimum impedance matching
  - Insufficient output power

- Many inductor - Large area

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Output impedance matching

If \( r_{ds} = \square \),

\[
Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{1}{j\omega C} \parallel (R_L + j\omega L)
\]

\( R_s \): source impedance (50\( \Omega \))

\( R_L \): inductor parasitic resistance

\[
V = V_{gs} + \frac{V_{gs}}{R_s} R_f
\]
\[
I = I_s + g_m V_{gs} = \left( \frac{1}{R_s} + g_m \right) V_{gs}
\]

\[
Z = \frac{V}{I} = \frac{R_f + R_s}{g_m R_s + 1}
\]
Output impedance matching

\[
Z_{\text{out}} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{1}{j\omega C} \parallel (R_L + j\omega L)
\]

\[
Z = \frac{1}{j\omega C} \parallel (R_L + j\omega L)
\]

\[
= \frac{1}{(R_L + j\omega L)} + j\omega C = \frac{R_L + j\omega(L - R_L^2C - \omega^2 L^2C)}{(1 - \omega^2 LC)^2 - \omega^2 R_L^2 C^2}
\]

(Calculation of resonance frequency)

\[
L - R_L^2C - \omega^2 L^2C = 0
\]

When \( \omega = \sqrt{\frac{1}{LC} - \left(\frac{R_L}{L}\right)^2} \), \( Z = \frac{L}{R_L C} \)

\[
\therefore Z_{\text{out}} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{L}{CR_L}
\]
Output impedance matching

\[ Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{L}{CR_L} \]

- Tune \( C \)
- Cancellation of an imaginary part
- Tune \( R_f \)
- Adjustment of a real part (50Ω)

\( Z_{out} \) depends on resonance frequency

\( Z_{out} \) can be matched 50Ω at arbitrary frequency

In fact, \( r_{ds} \) is small

- Cascode topology raises \( r_{ds} \)

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Schematic

- V_{DD} = 3.3V

Class-A bias & Differential topology for 3dB larger P_{sat}

- Change output matching band by switching C and R

- Isolators was removed by maintaining Z_{out} to 50Ω

Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{L}{CR_L}

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Chip micrograph

- TSMC 0.18 µm CMOS process
Measurement results are slightly shifted to lower frequency due to model inaccuracy
Measuring system

- Large signal measurement setup

- Input and output losses are measured separately, and are calibrated from results.

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Large signal measurement result

- **band 3 @ 7.5GHz**

- Measurement and simulation results agree with each other.
Large signal measurement result

\[ PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{dc}} \]

- \( P_{1\text{dB}} > 15.5 \text{ dBm} \)
- \( P_{\text{sat}} > 19.8 \text{ dBm} \)
- \( \text{PAE}_{1\text{dB}} > 4.7\% \)
- \( \text{PAE}_{\text{max}} > 7.1\% \)

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<table>
<thead>
<tr>
<th></th>
<th>Simulation</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>TSMC 0.18 (\mu)m CMOS</td>
<td></td>
</tr>
<tr>
<td><strong>(V_{DD})</strong></td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td><strong>(S_{22})</strong></td>
<td>&lt; -10 dB</td>
<td></td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>6.0~10.2 GHz</td>
<td>5.7~9.7 GHz</td>
</tr>
<tr>
<td><strong>(P_{1dB})</strong></td>
<td>17.6~19.4 dBm</td>
<td>16~19 dBm</td>
</tr>
<tr>
<td><strong>(P_{sat})</strong></td>
<td>20.9~22.0 dBm</td>
<td>20~22 dBm</td>
</tr>
<tr>
<td><strong>PAE_{peak}</strong></td>
<td>9.7~15.3 %</td>
<td>7~14 %</td>
</tr>
<tr>
<td><strong>Area</strong></td>
<td>Core size : 0.50 (\times) 0.39 (\times) 0.20 mm(^2)</td>
<td></td>
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</tbody>
</table>
### Comparison of CMOS PAs

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<thead>
<tr>
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<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
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<tbody>
<tr>
<td>Technology</td>
<td>0.09 µm</td>
<td>0.18 µm CMOS process</td>
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<td></td>
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<tr>
<td>$V_{DD}$ [V]</td>
<td>-</td>
<td>1.5</td>
<td>2.0</td>
<td>-</td>
<td>3.3</td>
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<tr>
<td>Frequency [GHz]</td>
<td>*5.2~13</td>
<td>6~10</td>
<td>3~10</td>
<td>3.7~8.8</td>
<td>5.74~9.68</td>
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<tr>
<td>$P_{1dB}$ [dBm]</td>
<td>-</td>
<td>**5</td>
<td>5.6~9.4</td>
<td>~15.6</td>
<td>15.5~19.2</td>
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<tr>
<td>$P_{sat}$ [dBm]</td>
<td>25.2</td>
<td>-</td>
<td>-</td>
<td>19</td>
<td>19.8~21.6</td>
</tr>
<tr>
<td>$\text{PAE}_{\text{peak}}$ [%]</td>
<td>21.6</td>
<td>17.6</td>
<td>-</td>
<td>25</td>
<td>7.1~14.0</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>***0.70</td>
<td>1.08</td>
<td>1.76</td>
<td>2.8</td>
<td>***0.20</td>
</tr>
</tbody>
</table>

* $S_{22} < -3\text{dB}$  ** Average $P_{1dB}$  *** Core size


Conclusion

- 6-10 GHz Multi-band tunable CMOS PA
  - For realization of single chip transceiver
  - To cover various standards
- Prototype of a CMOS PA
  - TSMC 0.18\(\mu\)m CMOS process
  - Using parallel resonance and resistive feedback
- Results
  - Frequency: 5.7 ~ 9.7 GHz
  - \(P_{1dB} > 15.5\) dBm, \(PAE_{peak} > 7.1\%\), Core size=0.20mm\(^2\)
  - The first tunable CMOS PA at 6-10GHz
Thank you for your attention.