Evaluation of a Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design

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SUMMARY An L-2L through-line de-embedding method has been verified up to millimeter wave frequency. The parasitics of the pad can be de-embedded by subtracting the parasitic matrix of the pad. Therefore, the de-embedding patterns, which is used for modeling active and passive devices, decrease greatly and the chip area also decreases. A one-stage amplifier is firstly implemented for helping verifying the de-embedding results. After that a four-stage 60 GHz amplifier has been fabricated in CMOS 65 nm process. Experimental results show that the four-stage amplifier realizes an input matching better than −10.5 dB and an output matching better than −13 dB at 61 GHz. A small signal power gain of 16.4 dB and a 1 dB output compression point of 4.6 dBm are obtained with a DC current consumption of 128 mA from a 1.2 V power supply. The chip size is 1.5 mm × 0.85 mm.

key words: CMOS amplifier, transmission line, millimeter wave, de-embedding, 60 GHz

1. Introduction

Nowadays many publications about millimeter wave (MMW) transceivers and its building blocks have been published both from academia and industry [1]–[9]. According to IEEE 802.15.3c a 9 GHz wide-band at 60 GHz can be used without license for Gbps wireless applications such as wireless personal area network (WPAN), wireless high definition multimedia interface (HDMI), point to point links and wireless personal area network (WPAN), wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links and wireless high definition multimedia interface (HDMI), point to point links. Accompanying with the scaling down of the CMOS technology, these single transistor and transistor with diode can be modeled from the L-2L through-line. Measurement results of the transistors, then a one-stage amplifier which is employed to verify the model. The implementation and measurement results of a four-stage amplifier are given in Sect. 4. Section 3 firstly describes the de-embedding results of the T-lines and the transistors, then a one-stage amplifier which is employed to verify the model. The implementation and measurement results of a four-stage amplifier are given in Sect. 4. Section 5 presents the final conclusion.

2. L-2L Through-Line De-Embedding Method

As shown in Fig. 1, two through-lines with a length of L and 2L have been utilized. The T-line can be decomposed into

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a cascade of five two-port networks consisting of the shunt parasitics of the pad, the intrinsic device and the series part of the pad as shown in Fig. 2. Therefore, the ABCD matrix of the T-line with a length of $l_i$ can be represented as the following product:

$$T_{m_i} = T_{pl}T_{sl}T_{l_i}T_{sr}T_{pr}$$

where

- $T_{l_i}$ represents the intrinsic line segment of structure $i$;
- $T_{pl}$ represents the parallel parasitics of the left pad;
- $T_{sr}$ represents the serial parasitics of the left pad;
- $T_{pr}$ represents the parallel parasitics of the right pad.

Let $T_{lpad} = T_{pl}T_{sl}$ and $T_{rpad} = T_{pr}T_{sr}$ represent the parasitic matrix of the left pad and the right pad, respectively. With $l_2 = 2l_1$, we can have

$$T_{m_1} = T_{lpad}T_{l_1}T_{rpad}$$
$$T_{m_2} = T_{lpad}T_{l_1}T_{l_1}T_{rpad}$$
$$T_{lpad}T_{rpad} = T_{m_1}T_{m_1}^{-1}T_{m_1} = T_{thru}$$

Converting $T_{thru}$ to Y-parameter $Y_{thru}$, the shunt parasitic and series parasitic can be expressed by

$$Y_{shunt} = Y_{pad}(1,1) + Y_{pad}(1,2)$$
$$Z_{series} = \frac{-1}{2Y_{pad}(1,2)}$$

So the ABDC matrix of $T_p$ and $T_s$ is given by

$$T_p = \begin{pmatrix} 1 & 0 \\ Y_{shunt} & 1 \end{pmatrix}$$
$$T_s = \begin{pmatrix} 1 & Z_{series} \\ 0 & 1 \end{pmatrix}$$

and

$$T_{lpad} = T_pT_s = \begin{pmatrix} 1 & 0 \\ 1 & 1 \end{pmatrix}
Y_{shunt}Z_{series} + 1$$
$$T_{rpad} = T_sT_p = \begin{pmatrix} 1 & 0 \\ 1 & Z_{series} \end{pmatrix}
Y_{shunt}$$

$$T_{thru} = \begin{pmatrix} 2Y_{shunt}Z_{series} + 1 & 2Z_{series} \\ 2Y_{shunt}(Y_{shunt}Z_{series} + 1) & 2Y_{shunt}Z_{series} + 1 \end{pmatrix}$$

Therefore, the ABCD matrix of the DUT can be obtained by

$$T_{dut} = T_{lpad}^{-1}T_{meas}T_{rpad}^{-1}$$

Figure 3 shows the de-embedding procedure.

Through-only de-embedding method also models the parasitics of the pad by using lumped components. When the length of the through-line is zero for the ideal case, the result of through-only de-embedding method is the same as that of the L-2L through-line de-embedding method. However as the length becomes longer the error becomes remarkable to treat the through-line as a lumped component. A T-line is de-embedded to evaluate the accuracy of the through-only de-embedding method. The characteristic impedance $Z_c$, attenuation constant $\alpha$ and phase constant $\beta$ of the T-line have been calculated with the length change of the through-line. The calculation result is shown in Fig. 4. The error term $\Delta$ is given by

$$\Delta = \frac{|X^L - 2l - X^L|}{X^L}$$
where $L$ is the length of the de-embedded T-line and $l$ half of the length of the through-line. $X^2$ is the de-embedded results when $l = 0$. Term $X$ represents the characteristics impedance $Z_c$, attenuation constant $\alpha$ and phase constant $\beta$ of a T-line. The value of $L$, $Z_c^2$, $\alpha^2$ and $\beta^2$ are 400 $\mu$m, 45 $\Omega$, 1 dB/mm and 114.5 deg/mm, respectively. Figure 4 shows that $\Delta \alpha$ and $\Delta \beta$ is zero while the error term $\Delta Z_c$ increases as $l$ increasing and has a 3% difference when $l$ is 50 $\mu$m. The detail of the calculation is given in the Appendix.

3. De-Embedding Experimental Results

3.1 Transmission Lines De-Embedding

Two kinds of T-lines have been implemented in CMOS 65 nm process. The structure of the T-lines is shown in Fig. 5. Slow-wave coplanar waveguide (SWCPW) T-lines use Metal 1 as shield. Due to the design rule Metal 1 can not shield the substrate totally. CPWs with two-metal ground T-lines use Metal 1 and Metal 2 as shield. Metal 1 and Metal 2 are interleaved in parallel with the waveguide metal and connected in the direction perpendicular to the waveguide metal, which shield the substrate totally. SWCPW T-lines are employed to extract the parasitics of the pad by using the L-2L through-line method. After the pad is modeled, CPWs with two-metal ground have been de-embedded by eliminating the parasitics of the pad. The chip micrograph of the T-lines is shown in Fig. 6. De-embedding has been carried out in different ways for comparing. By using the method specified in [16] the characteristics of the CPWs with two-metal ground can be calculated from the S-parameters. Figure 7 shows the de-embedded result by using the OS de-embedding method. As can be seen, the characteristic impedance $Z_0$ has a large difference at high frequency which are supposed to be identical. The de-embedding results by using through-only method are given in Fig. 8. As shown that the characteristic impedance and phase constant are matched very well for 200-$\mu$m and 400-$\mu$m CPWs with two-metal ground. However, the attenuation have large difference beyond 20 GHz. The reason is considered as the coupling between the probes since the length of the through pattern is only 40 $\mu$m. Figure 9 gives the de-embedded results by using the L-2L through-line method. Although there is little difference when the frequency is beyond 80 GHz, good matches have been realized for the 200-$\mu$m and 400-$\mu$m T-lines. Therefore the T-lines can be modeled accurately based on the de-embedding results.

3.2 Transistor De-Embedding

Transistors have also been implemented in CMOS 65 nm process. T-Lines are employed for the access lines of the transistors which can be de-embedded after modeling the T-lines. The micrograph are shown in Fig. 10. The Y-matrix and Z-matrix of the pad are subtracted from the measured matrix of the transistors. The access T-lines are also de-embedded. The maximum stable gain (MSG) and maximum available gain (MAG) of a transistor after de-embedding is given in Fig. 11. The finger width of the transistor is 2 $\mu$m and the total width 40 $\mu$m.
3.3 One-stage Amplifier

To verify the precision of the de-embedding method and the model of the T-line, a one-stage amplifier has been fabricated in CMOS 65 nm process. The schematic and micrograph are shown in Fig. 12. A 5.4 dB power gain at 67 GHz has been realized at a $V_{gs}$ of 0.8 V and a $V_{ds}$ of 1.2 V. The measured MSG of the transistor is about 9.4 dB as shown in Fig. 11. Therefore the loss of the matching network is about 4 dB. The measured and simulated results including pads are compared in Fig. 13. As can be seen that the simulation results before de-embedding does not match with the measurement results. However, the simulation results after de-embedding match with the measurement results very well.

Fig. 8 Through-only de-embedding method for 200-μm and 400-μm CPWs with two-metal ground. (a) Characteristic impedance. (b) Attenuation constant. (c) Phase constant.

Fig. 9 L-2L through-line de-embedding method for 200-μm and 400-μm CPWs with two-metal ground. (a) Characteristic impedance. (b) Attenuation constant. (c) Phase constant.

Fig. 10 Micrograph of the transistor.
even though the peak of $S_{11}$ and $S_{22}$ shifts about 2–3 GHz. There are several reasons which are considered responsible for that: (1) Inaccuracy of the DC supply impedance; (2) Modeling error related to the Tee junction and the decoupling MIM model; (3) Variation of the DC-cut capacitance. Because to model the Tee-junction accurately, a three-port test element is needed. However, due to the lack of measurement instruments, we can not measured it up to 110 GHz. Therefore, a two-port test element is utilized. As to the de-coupling MIM model, because the characteristic impedance are very low, it is very sensitive to the measurement.

4. Design and Measurement Results of 4-Stage CMOS PA

By using the built models in Sect. 3 a four-stage amplifier has been designed and fabricated in CMOS 65 nm process. The measured T-lines are employed for the matching blocks. The first three stages are designed to realize a better gain matching, whereas the final output stage is optimized for a power matching. The load impedance is obtained from a load-pull analysis.

The circuit schematic of the 4-stage CMOS power amplifier is given in Fig. 14 and Fig. 15 shows the micrograph. The chip size is $1.5 \text{ mm} \times 0.85 \text{ mm}$. Figures 16 shows the measured and simulated S-parameters. A measured small signal power gain of 16.4 dB is obtained which is about 1.1 dB smaller than the simulated one. The reason is considered as that the non-ideal ground degenerates the source of the transistors and therefore decreases the power gain. The large signal measurement results are shown in Fig. 17. The simulation results are about 0.6 dB larger than the measurement ones. The difference can be generated from the large signal (DC) model of the transistor. And the 1 dB output compression point of 4.6 dBm at 61.5 GHz with a DC current consumption of 128 mA at a VDD of 1.2 V.

Table 1 shows the summary of the presented and conventional 60 GHz CMOS power amplifiers. The MMW CMOS power amplifier reported in this paper achieves state-of-the-art performance.
Fig. 14  Circuit schematic of the four-stage power amplifier.

Fig. 15  Micrograph of the four-stage PA.

Fig. 16  Measured and simulated S-parameters results of the four-stage amplifier. (a) $S_{11}$ and $S_{22}$ with markers at 61 GHz. (b) $S_{21}$.

Fig. 17  Large signal characteristics of the four-stage PA. (a) Output power versus input power. (b) Large signal power gain versus input power.

5. Conclusion

An L-2L through-line de-embedding method has been verified up to millimeter wave frequency. The parasitics of the pad can be modeled from the L-2L through-line. Measurement results of the transmission lines and transistors can be de-embedded by subtracting the parasitic matrix of the pad. Therefore, the de-embedding patterns decrease greatly and the chip area also decreases which is used for modeling active and passive devices. A one-stage amplifier is firstly implemented for helping verifying the de-embedding results.
After that a four-stage 60 GHz amplifier has been fabricated in CMOS 65 nm process. Experimental results show that the four-stage amplifier realizes an input matching better than −10.5 dB and an output matching better than −13 dB at 61 GHz. A small signal power gain of 16.4 dB and a 1 dB output compression point of 4.6 dBm are obtained with a DC current consumption of 128 mA from a 1.2 V power supply. The chip size is 1.5 mm × 0.85 mm.

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References

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\[
\text{T} = \text{T}_{\text{thru}} \cdot \text{T}_{\text{line}} \cdot \text{T}_{\text{pad}} = \left( \begin{array}{ccc} A & B \\ C & D \end{array} \right)
\]

(A-1)

where \( T_{\text{thru}} \) is the measured through-only pattern ABCD matrix and \( t \) is the half length of the through-line.

Appendix

As shown in Fig. A-1, the ABCD matrix of the through-only pattern can be expressed by

\[
\text{T}_{\text{thru}} = \text{T}_{\text{pad}} \cdot \text{T}_{\text{line}} \cdot \text{T}_{\text{pad}} = \left( \begin{array}{ccc} A & B \\ C & D \end{array} \right)
\]

(A-1)

where \( T_{\text{thru}} \) is the measured through-only pattern ABCD matrix and \( t \) is the half length of the through-line.

\[
\text{T}_{\text{pad}} = \left( \begin{array}{c} 1 \\ Y_{\text{shunt}} \end{array} \right) \left( \begin{array}{c} Z_{\text{series}} \\ Y_{\text{shunt}} \cdot Z_{\text{series}} \cdot 1 \end{array} \right) = \left( \begin{array}{c} 1 \cdot Z_{\text{series}} + 1 \\ Y_{\text{shunt}} \cdot Z_{\text{series}} \cdot 1 \end{array} \right)
\]

(A-3)

\[
\text{T}_{\text{line}} \left( \begin{array}{c} \cosh(y) \\ \sinh(y) \end{array} \right) = \left( \begin{array}{c} Z_{\text{c}} \sinh(y) \\ \cosh(y) \end{array} \right)
\]

(A-4)

\[
\text{A} = (2Y_{\text{shunt}}Z_{\text{series}} + 1) \cdot \cosh(y) + \sinh(2y) \cdot \cosh(y)
\]

(A-5)
The Y matrix of the through-only pattern can be obtained by using the through-only method is expressed as

\[
\begin{align*}
Y_{\text{shunt}} &= Y_{11} + Y_{12}, \\
Z'_{\text{series}} &= -\frac{1}{Y_{12}}.
\end{align*}
\]  
(A-18)

(A-19)

Therefore the ABCD matrix of the pad calculated by using the through-only method is given by

\[
\begin{align*}
T'_{\text{pad}} &= \begin{pmatrix}
1 & Z'_{\text{series}} \\
Y_{\text{shunt}} & Y_{\text{shunt}} Z'_{\text{series}} + 1
\end{pmatrix}, \\
T'_{\text{dut}} &= \begin{pmatrix}
1 & 0 \\
0 & 1
\end{pmatrix} \cdot T_{\text{meas}} \cdot \begin{pmatrix}
1 & 0 \\
0 & 1
\end{pmatrix}^{-1}.
\end{align*}
\]  
(A-20)

(A-21)

The DUT can be de-embedded by using the following expression.

\[
T_{\text{dut}} = T'_{\text{pad}} \left( \begin{pmatrix}
1 & Z'_{\text{series}} \\
Y_{\text{shunt}} & Y_{\text{shunt}} Z'_{\text{series}} + 1
\end{pmatrix}
\right) T_{\text{meas}} \left( \begin{pmatrix}
1 & 0 \\
0 & 1
\end{pmatrix}
\right)^{-1}.
\]  
(A-22)

Transferring the ABCD matrix to S matrix and using the method specified in [16] the characteristics of the T-line can be calculated from the S-parameters.

\[
\gamma = \alpha + j\beta
\]  
(A-23)

\[
e^{-\gamma(L-2l)} = \left( \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right)^{-1}.
\]  
(A-24)

where \(L\) is the length of the T-line,

\[
K = \left( \frac{(S_{11}^2 - S_{21}^2 - 2S_{12}^2)^2}{(2S_{21})^2} \right)^{\frac{1}{2}}.
\]  
(A-25)

\[
Z = Z_0 \left( \frac{1 + S_{11}^2 - S_{21}^2}{1 - S_{11}^2 - S_{21}^2} \right)^{\frac{1}{2}}.
\]  
(A-26)

where \(Z_0\) is 50 \(\Omega\).

Changing the length of the through-only pattern, the characteristic impedance, attenuation constant and phase constant have been calculated. The calculated results is shown in Fig. 4 in Sect. 2.

So the shunt admittance and series impedance calculated by using the through-only method is expressed as

\[
Y_{\text{shunt}} = Y_{11} + Y_{12},
\]

\[
Z'_{\text{series}} = -\frac{1}{Y_{12}}.
\]

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