A $484\mu m^2$, 21GHz LC-VCO Beneath a Stacked-Spiral Inductor

Rui Murakami, Kenichi Okada, and Akira Matsuzawa

Tokyo Institute of Technology, Japan
Contents

- Background
- Downsizing of LC-VCO
- Circuit Stacking Beneath the Inductor
- Measurement Result
- Summary
As supply voltage is scaled down, low voltage circuits are needed.
Jitter (Phase noise) of Oscillators

- LC-VCO [1]

\[
L_{LC} = \frac{\omega_0^2}{\omega_{offset}^2} \cdot \frac{kT}{V_{DD}I_{bias}} \cdot \frac{1 + \gamma_n}{Q^2}
\]

- Ring-VCO [2]

\[
L_{Ring} = \frac{\omega_0^2}{\omega_{offset}^2} \cdot \frac{kT}{V_{DD}I_{bias}} \cdot 2M \left\{ \frac{V_{DD}}{V_{DD} - V_{TH}} (\gamma_n + \gamma_p) + 1 \right\}
\]

- Ring oscillators are more susceptible to the effect of downscaling the supply voltage.


k: Boltzmann’s constant
T: Absolute temperature
\(f_0\): freq.
\(f_{offset}\): Offset freq.
\(V_{TH}\): Threshold voltage
M: Number of stages
Q: Quality factor of LC-tank
I_{bias}: Bias current
\(\gamma_n\), \(\gamma_p\): Noise factor

[Image]
Problem of Clock Generator

Ring-VCOs must be replaced with LC-VCOs

## Comparison of Oscillators

<table>
<thead>
<tr>
<th></th>
<th>Ring</th>
<th>LC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bad</td>
<td></td>
<td>Good</td>
</tr>
<tr>
<td>Large</td>
<td>Noise</td>
<td>Small</td>
</tr>
<tr>
<td>@high freq.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Very small</td>
<td>Area</td>
<td>Large</td>
</tr>
</tbody>
</table>

To replace Ring-VCO by LC-VCO
Increasing chip area will become a problem.

A very small LC-VCO is desired.

The inductor occupies the dominant area in a LC-VCO.

It is needed to miniaturize the Inductor
Oscillation Frequency

\[ \text{frequency} = \frac{1}{2\pi \sqrt{LC}} \]

At a higher frequency, smaller inductance is needed. VCO can be designed using a small inductor.

Over 20GHz, quality factor degradation is caused by the skin effect.

- Poor phase noise and high power consumption.

A 20GHz LC-VCO results in a good balance between area and phase noise.
Stacked-spiral Inductor

- Single layer
- Wide line width
- Large diameter
- Low R, High Q
- Large area

Mono-layer inductor

- Multi layer
- Narrow line width
- Small diameter
- High R, Low Q
- Ultra low space

Stacked-spiral inductor
Comparison the Inductors

Stacked-spiral

Mono-layer

15µm

1/44

Area

100µm

<table>
<thead>
<tr>
<th></th>
<th>@20GHz</th>
<th>$L_S$ [nH]</th>
<th>$R_S$ [Ohm]</th>
<th>$C_L$ [fF]</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stacked-spiral</td>
<td></td>
<td>1.16</td>
<td>51.7</td>
<td>9.76</td>
<td>2.82</td>
</tr>
<tr>
<td>Mono-layer</td>
<td></td>
<td>0.51</td>
<td>4.19</td>
<td>18.6</td>
<td>15.5</td>
</tr>
</tbody>
</table>
Placement of Core-circuit

When the Inductor is miniaturized, the core-circuit size becomes close to the area of the inductor.

Insert core-circuit under the inductor.

Inductive coupling is a problem.
Inductive Coupling

Inductance and quality factor will be degraded by inductive coupling

\[ M = 2m \ln \left( \frac{m}{d} + \sqrt{1 + \frac{m^2}{d^2}} \right) + \frac{d}{m} - \sqrt{1 + \frac{d^2}{m^2}} \]

\[ L = L_1 \left( 1 - \frac{k^2 \omega^2 L_2^2}{R^2 + \omega^2 L_2^2} \right) = L_1 \left( 1 - \frac{k^2 Q_2^2}{1 + Q_2^2} \right) \]

Reducing coupling

To reduce coupling, some layout techniques are applied.

- Slit shaping interconnections
- Placing inductor trace and interconnections orthogonally
Analysis of Interconnection Effects

The model of the interconnections is created and simulated the influence on $L_S$ and $Q$ by HFSS.

<table>
<thead>
<tr>
<th></th>
<th>$L_S$ [nH]</th>
<th>$Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>1.16</td>
<td>2.82</td>
</tr>
<tr>
<td>Beneath</td>
<td>1.14</td>
<td>2.67</td>
</tr>
</tbody>
</table>

$L_S$ 3%, $Q$ 5% down

It corresponds 0.4dB in FoM.
Chip Micrograph(1)

CMOS 65nm

Output Buffer

VCO core

22 µm

22 µm
Chip Micrograph (2)

VCO core
100µm
100µm
Measurement Result

$$FoMA = -\left( \mathcal{L}\{\Delta f\} - 20 \log\left( \frac{f_o}{\Delta f} \right) + 10 \log\left( \frac{P_{DC}}{1 \text{mW}} \right) \right) - 10 \log\left( \frac{\text{Area}}{1 \text{mm}^2} \right)$$ [5]


2010/09/28  R.Murakami, Tokyo Tech
## Performance Summary

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>173</td>
<td>173</td>
<td>154</td>
<td>190</td>
</tr>
<tr>
<td>FoM</td>
<td>173</td>
<td>173</td>
<td>154</td>
<td>190</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Summary

• A very compact LC-VCO with a stacked-spiral inductor and the core-circuit being placed beneath the inductor is proposed.

• To reduce coupling, interconnections are slit shaped and orthogonalized with the coil trace.

• This VCO achieves a chip area of $484\,\mu m^2$ equaling ring-oscillator and FoMA of 206dBc/Hz.
Thank you!!