A 0.5 V, 1.2 mW, 160 fJ, 600 MS/s 5 bit Flash ADC

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Outline

- Motivation
- Design Concept
- Calibration Technique
- Measurement Results
- Conclusions
Motivation

• An ultra-low power ADC is strongly required.
  – Portable applications
  – Ubiquitous wireless sensor system
  – Green IT

• A low voltage operation is required for further technology scaling and low power operation.
  – Analog circuits design becomes more difficult.
    • Increasing $V_T$ mismatch
    • Degradation of gain and distortion of an amplifier
  – The FoM of an ADC should be reduced like digital circuits.
    • Optimizing a speed, resolution and power.
    • Calibration technique for low voltage operation.
Performance of flash ADCs

FoM is deteriorated by the offset voltage of the comparator. Offset voltage should be low at low voltage operation.

\[
\Delta ENOB = \frac{1}{2} \log_2 \left( 1 + 12 \left( \frac{V_{\text{off}}(\sigma)}{V_q} \right)^2 \right)
\]

\[
\text{FoM} = \frac{P_d}{f_c \times 2^{N - \Delta ENOB}}
\]

\(V_{\text{off}}(\sigma)\): Offset voltage

\(V_q\): 1LSB voltage
FoM vs. VDD

FoM can be significantly reduced by reducing power supply voltage VDD.

\[
\text{FoM} = \frac{f_c \times E_c \times 2^N}{f_c \times 2^{N-\Delta \text{ENOB}}} = E_c 2^{\Delta \text{ENOB}}
\]

\[
E_c = C_c V_{DD}^2 + \frac{V_{DD} \cdot I_c \exp\left(-\frac{V_T}{S}\right)}{f_c}
\]

\(E_c: \text{Energy consumption for each comparator and followed logic circuits.}\)
FoM delay product

The FD product suggests the balance between the number of interleaving and decrease of energy consumption.

\[ FD = FoM \times \text{Delay} \]

Excessive number of Interleaving ADC

- Large area
- Driving difficulty
- Reduction of ENOB

Delay time

\[ T_d = k \frac{V_{DD}}{(V_{DD} - V_T)^\alpha} \]
Forward body biasing can decrease the delay time \((1/2)\) and can be used easily at 0.5 V operation.

Increased leakage current in the proposed ADC is 0.32 mA by forward body biasing.
Proposed Calibration Technique

**Conventional Calibration**
(Capacitor DAC base[5])
- MOS varactor sensitivity $\downarrow$
- Delay time and power $\uparrow$

**Proposed Calibration**
(Timing control base)

$$V_{DD}=0.5V, \quad f_s=500MHz$$

<table>
<thead>
<tr>
<th></th>
<th>no CAL</th>
<th>Cap CAL [5]</th>
<th>Proposed</th>
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<tbody>
<tr>
<td>$V_{off}(\sigma)$ [mV]</td>
<td>10.1</td>
<td>5.79</td>
<td>1.49</td>
</tr>
<tr>
<td>$P_d$ [$\mu$W]</td>
<td>14.5</td>
<td>21.4</td>
<td>24.5</td>
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<tr>
<td>Delay [ps]</td>
<td>365</td>
<td>756</td>
<td>511</td>
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</table>

ADC Structure

90nm 1P9M CMOS process

S/H
Comparator ×4
Up Down
Counter 6b ×4

S/H
Comparator ×4
Up Down
Counter 6b ×4

Comparators Block (32 Comparators)

Reference ladder

2b Interpolation

Error Correction Circuit

Thermometer to Binary Encoder

5b Flip Flops

Clock Divider

$V_{in}$

$\phi$

$\phi/4$

$D_{out}$

$\phi/8$
DNL and INL

DNL

\[ \pm 2.2 \text{ LSB} \Rightarrow \pm 0.5 \text{ LSB}. \]

INL

\[ \pm 1.5 \text{ LSB} \Rightarrow \pm 0.3 \text{ LSB}. \]

(Measurement results are updated because the measurement setup is improved.)
SFDR and SNDR vs. Fsample

Fin = 1 MHz

SFDR, W/ CAL
SFDR, W/O CAL
SNDR, W/ CAL
SNDR, W/O CAL

Sampling Frequency [MSps]
SFDR and SNDR vs. Fin

Fs\textsubscript{sample} = 360 MSps

\textbf{FoM\textsubscript{Best}} = 110 fJ/conv.
# Performance Summary

<table>
<thead>
<tr>
<th>Reference #</th>
<th>[7]</th>
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<th>[9]</th>
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<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (bit)</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
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<tr>
<td>$fs$ (GS/s)</td>
<td>0.5</td>
<td>1.75</td>
<td>1.75</td>
<td>0.06</td>
<td>0.6</td>
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<tr>
<td>SNDR (dB)</td>
<td>26</td>
<td>30</td>
<td>30</td>
<td>26</td>
<td>27</td>
</tr>
<tr>
<td>$P_d$ (mW)</td>
<td>5.9</td>
<td>2.2</td>
<td>7.6</td>
<td>1.3</td>
<td>1.2</td>
</tr>
<tr>
<td>Active area (mm$^2$)</td>
<td>0.87</td>
<td>0.017</td>
<td>0.03</td>
<td>-</td>
<td>0.083</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>1.2</td>
<td>1</td>
<td>1</td>
<td>0.6</td>
<td>0.5</td>
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<tr>
<td>FoM (fJ)</td>
<td>750</td>
<td>50</td>
<td>150</td>
<td>1060</td>
<td>160</td>
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<tr>
<td>CMOS Tech. (nm)</td>
<td>65</td>
<td>90</td>
<td>90</td>
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<tr>
<td>Architecture</td>
<td>SAR</td>
<td>Fold+Flash</td>
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</table>

$FoM_{Fmax} = 160fJ @ 600MSps$

$FoM_{Best} = 110 \text{ fJ} @ 360MSps$

Conclusions

• The strategy for low voltage operation is proposed.
  – FoM delay product (FD) is considered for not only low FoM but also high speed operation.

• Low voltage design techniques are proposed.
  – Forward body bias can be used easily at 0.5 V operation. ($T_d \Rightarrow 1/2$)
  – The timing control based offset calibration technique is proposed. (DNL / INL 2 LSB => 0.5 LSB)

• Proposed ADC has good power efficiency and high speed operation.
  – 600MSps, ERBW = 200 MHz, ENOB = 4.6 bit, $\text{FoM}_{\text{Best}} = 110$ fJ/ conv. at 0.5 V supply.
Thank you for your interest!

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