Phase Noise Scaling of LC-VCO for Ultra Low Supply Voltage

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Outline

• Background
  - Clock generation in System-on-Chip

• Challenging
  - Supply voltage scaling

• Low voltage clock generator’s issues
  - Ring VCO becomes infeasible due to too large phase noise performance

• Possible solution

• Conclusion
Research Background

- Cellular
- Appliance
- Radar
- WLAN
- DAB
- WiMax
- RFID
- GPS
- UWB

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Clock generation circuits are widely used in a number of applications in which a reference tone is required.
How to Evaluate Clock Generator?

- **Phase noise**
  - Measure of spectral density in frequency domain
  - Units: dBC/Hz (decibels below the carrier per Hz)

- **Jitter** *(Better choice for clock)*
  - Measurement of variations in time domain
  - Units: Seconds (usually pS)
What is Jitter in Clock Generator?

- Waveform transition is too early
- Waveform transition is too late

**Ideal waveform**

**Jitter**

Timing variation in signal waveform

**Cause of Jitter (phase noise):** Thermal noise and shot noise
How Jitter Affect Performance?

Clock generator with small jitter (phase noise) is strongly desired.
How about phase noise performance along with supply voltage scaling?
Phase Noise Comparison

**LC-VCO** [A. Mazzanti, et al., JSSC 2008]
\[
\frac{\omega_0^2}{\omega_{\text{offset}}^2} \cdot \frac{kT}{V_{\text{DD}}I_{\text{bias}}} \cdot \frac{1 + \gamma_n}{Q^2}
\]

**Ring-VCO** [A. Abidi, JSSC 2006]
\[
\frac{\omega_0^2}{\omega_{\text{offset}}^2} \cdot \frac{kT}{V_{\text{DD}}I_{\text{bias}}} \cdot 2M \left\{ \frac{V_{\text{DD}}}{V_{\text{DD}} - V_{\text{TH}}} \left( \gamma_n + \gamma_p \right) + 1 \right\}
\]

M: #stages

\[ V_{\text{TH}} = \frac{V_{\text{DD}}}{4}, \quad \gamma_n = \gamma_p = \frac{2}{3}, \quad M = 3, \quad Q = 10 \]

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Scaling of Jitter

With same power consumption, LC-VCO has much smaller jitter performance

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# Scaling of Phase Noise

<table>
<thead>
<tr>
<th>$V_{DD}$</th>
<th>Type</th>
<th>$P_{DC}$</th>
<th>Phase Noise +10dB margin @1MHz</th>
<th>Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2-V (Now)</td>
<td>LC</td>
<td>1mW</td>
<td>-121.6 dBc/Hz</td>
<td>0.16ps</td>
</tr>
<tr>
<td></td>
<td>Ring</td>
<td>1mW</td>
<td>-91.6 dBc/Hz</td>
<td>5.0ps</td>
</tr>
<tr>
<td>0.5-V (Future)</td>
<td>LC</td>
<td>0.17mW</td>
<td>-114.0 dBc/Hz</td>
<td>0.38ps</td>
</tr>
<tr>
<td></td>
<td>Ring</td>
<td>0.17mW</td>
<td>-84.0 dBc/Hz</td>
<td>12.0ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>174mW</td>
<td>-114.0 dBc/Hz</td>
<td>0.38ps</td>
</tr>
</tbody>
</table>

For 0.5-V clock generators, ring-VCO becomes infeasible due to large power consumption and/or large jitter.
Comparison of Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Jitter</th>
<th>$P_{DC}$</th>
<th>Area</th>
<th>Tuning range</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5-V Ring VCO</td>
<td>Very Bad</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>0.5-V LC VCO</td>
<td>Very Good</td>
<td>Fair, but can be improved</td>
<td>Fair, and improved in [1]</td>
<td>Fair, but can be improved</td>
</tr>
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</table>

LC-VCO with $P_{DC}$, area and tuning range optimization is necessary for 0.5-V clock generation circuits

Research Status

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Topology</td>
<td>-</td>
<td>LC</td>
<td>LC</td>
<td>LC</td>
<td>LC</td>
<td>Ring</td>
</tr>
<tr>
<td>V_{DD}</td>
<td>V</td>
<td>0.6</td>
<td>0.5</td>
<td>0.9</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Frequency</td>
<td>GHz</td>
<td>5.3 ~ 6</td>
<td>3.65 ~ 3.76</td>
<td>2.17 ~ 2.73</td>
<td>2.15~2.62</td>
<td>0.12-1.3</td>
</tr>
<tr>
<td>Tuning range</td>
<td>%</td>
<td>8.1</td>
<td>3</td>
<td>22.8</td>
<td>20</td>
<td>85</td>
</tr>
<tr>
<td>Jitter</td>
<td>ps</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&gt;15</td>
</tr>
</tbody>
</table>


Ultra-low-voltage clock generator with **wide tuning range** (merit of ring VCO) and **sub-picosecond-jitter** (merit of LC VCO) are desired in future 0.5-V SoC and power aware SoC.

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Possible Solution

Conventional

Proposed

[REF]: Wei Deng, Kenichi Okada, and Akira Matsuzawa "A 0.5-V, 0.05-to-3.2 GHz, 4.1-to-6.4 GHz LC-VCO Using E-TSPC Frequency Divider with Forward Body Bias for Sub-Picosecond -Jitter Clock Generation“ to be presented at Asian Solid-State Circuits Conference (A-SSCC), Nov. 2010
Summary

• Lowering of supply voltage is required to realize low-active-power circuits.

• Phase noise (Jitter) will become larger according to the voltage scaling.

• Ring-VCO become infeasible due to too large phase noise (jitter) and/or too large power consumption.

• To reduce the power consumption of the clock generator, adoption of LC-VCOs is an unavoidable way in such low-voltage condition.
Toward the Future

• Ultra-low-voltage LC-VCO offers tremendous opportunities in phase noise (jitter) performance of clock generator in SoC design.

• The tuning range of ultra-low-voltage LC-VCO should be improved to fulfill the requirement for future 0.5-V sub-picosecond-jitter clock generation.
Thanks for your attention!

Q & A