A 0.114-mW Dual-Conduction Class-C CMOS VCO with 0.2-V Power Supply

K. Okada, Y. Nomiyama, R. Murakami, and A. Matsuzawa

Tokyo Institute of Technology, Japan

2009/6/18, VLSI Circuits, Kyoto
Outline of Presentation

• Motivation
  – Supply voltage scaling
  – Jitter degradation

• Low-voltage VCO’s issues

• The proposed Dual-Conduction topology
  – Low-power and Low-phase noise
    with a very low supply voltage

• Measurement results

• Conclusions
The voltage scaling is required again. Low-voltage circuit design is challenging.
Phase Noise Comparison

**LC-VCO [A.Mazzanti, et al., JSSC 2008]**

\[ \frac{\omega_0^2}{\omega_{\text{offset}}^2} \cdot \frac{kT}{V_{\text{DD}} I_{\text{bias}}} \cdot \frac{1 + \gamma_n}{Q^2} \]

+30dB worse

**Ring-VCO [A.Abidi, JSSC 2006]**

\[ \frac{\omega_0^2}{\omega_{\text{offset}}^2} \cdot \frac{kT}{V_{\text{DD}} I_{\text{bias}}} \cdot 2M \left\{ \frac{V_{\text{DD}}}{V_{\text{DD}} - V_{\text{TH}}} \left( \gamma_n + \gamma_p \right) + 1 \right\} \]

M: #stages

\[ V_{\text{TH}} = \frac{V_{\text{DD}}}{4}, \quad \gamma_n = \gamma_p = \frac{2}{3}, \quad M = 3, \quad Q = 10 \]
With the same power consumption, LC-VCO has much smaller jitter performance.
Clock Generation with Low Vdd

- Lowering of supply voltage is required to realize high-speed and low-active-power circuits.
- Jitter will become larger according to the voltage scaling.
- Ring-VCO become infeasible due to too large jitter or too large power consumption.
- To reduce the power consumption of the clock generator, use of LC-VCOs is an unavoidable way in such the low-voltage condition.
Low-Voltage LC-VCO

- Transformer-Feedback VCO can operate with a low supply voltage.
- 0.5V and 0.35V VCOs are reported.
  
  [1] K. Kwok, and H. C. Luong, JSSC 2005

- **Class-C VCO** archives 196dBc/Hz of FoM.
- Startup is an issue of Class-C VCO under the low-voltage condition.

Summary of This Work

- Sub-0.5V LSI
- A Dual-Conduction topology is proposed for Class-C VCO in this work.
- It is modified to work with a very low supply voltage.
- 0.2V VCO is realized by using a 0.18μm CMOS process with 114μW of power consumption.
Impulse Sensitivity Function (ISF)

Voltage Waveform

Case 1

Case 2

Phase is NOT shifted

Phase is shifted

Ideal Current Conduction

Ideal Current

Conventional LC-VCO
Current Conduction of Class-C VCOs

ISF

Ideal Current

Class-C VCO
Current Conduction of Class-C VCOs

Class-C VCO

Dual-Conduction
Class-C VCO
(This work)
**Class-C VCO** \[2\]

\[ V_{eff} = V_{gs} - V_{th} \]

Conventional LC-VCO

\[ V_{eff} = V_{gs} - V_{th} \]

Class-C VCO

Condition for Class-C Operation

\[ V_{ds} \]

\[ V_{DD} \]

\[ 0 \]

\[ -\pi \]

\[ -\pi/2 \]

\[ 0 \]

\[ \pi/2 \]

\[ \pi \]

\[ \phi \text{[rad.]} \]

Active region: \( V_{ds} > V_{eff} \)

\[ V_{eff} = V_{gs} - V_{th} \]

\[ -V_{od} = V_{gbias} - V_{th} \]
Issue of Class-C VCO for Low Vdd

\[ V_{dd} \quad V_{dc} \quad S \quad S \quad S \]

\[ \phi [\text{rad.}] \]

\[ V_{od} \] has to be small due to the start-up problem, so conduction angle cannot be reduced.

\[ V_{eff} = V_{gs} - V_{th} \]

\[ = V_{gbias} - V_{th} \]
Dual-Conduction Class-C VCO (Proposed)

for Class-C operation

for start-up

$I_{ds1}$

$V_{od1} > 0$

$I_{ds2}$

$V_{od2} \approx 0$
Dual-Conduction Current Waveform

\[ V_{od1} = 0.12V \ (\Phi_1 = 0.2\pi) \]
\[ V_{od2} = 0V \ (\Phi_2 = 0.5\pi) \]
Comparison of Current Waveforms

Dual Conduction realizes a narrower current waveform.

\( \Phi_0 = 0.4\pi \)

Single Conduction (conventional)

\( \Phi = 0.5\pi \) & \( 0.2\pi \)

\( I_{ds1} + I_{ds2} \)

Dual Conduction (proposed)
**Analytical Comparison**

**Single Conduction**
(conventional)

- $V_{od} = 0.05V$ ($\Phi_0 = 0.4\pi$)
- $PN = -106\text{dBc/Hz-1MHz}$
- $P_{dc} = 168\mu W$
- $FoM = 188\text{dBc/Hz}$

**Dual Conduction**
(proposed)

- $V_{od1} = 0.12V$ ($\Phi_1 = 0.2\pi$)
- $V_{od2} = 0V$ ($\Phi_2 = 0.5\pi$)
- $PN = -109\text{dBc/Hz-1MHz}$
- $P_{dc} = 162\mu W$
- $FoM = 191\text{dBc/Hz}$

(*) $V_{dd} = 0.2V$, $A = 0.15V$, $V_{th} = 0.5V$, $f_0 = 5GHz$, $Q = 10$
Chip Micrograph

- 0.18\(\mu\)m CMOS process
- 670\(\mu\)m x 440\(\mu\)m for core area
Phase Noise Measurement

V_{gbias1}=0.45, V_{gbias2}=0.55, f_0=4.5\text{GHz}

-104\text{dBc/Hz}@1\text{MHz} for 0.2\text{V}
-109\text{dBc/Hz}@1\text{MHz} for 0.3\text{V}
## Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>[2]</th>
<th>[1]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.13μm CMOS</td>
<td>0.18μm CMOS</td>
<td>0.18μm CMOS</td>
</tr>
<tr>
<td>Vdd [V]</td>
<td>1.0</td>
<td>0.5</td>
<td>0.3</td>
</tr>
<tr>
<td>PDC [mW]</td>
<td>1.3</td>
<td>0.57</td>
<td>0.159</td>
</tr>
<tr>
<td>$f_0$ [GHz]</td>
<td>4.9</td>
<td>3.8</td>
<td>4.5</td>
</tr>
<tr>
<td>Phase noise [dBc/Hz]</td>
<td>-130 @3MHz</td>
<td>-119 @1MHz</td>
<td>-109 @1MHz</td>
</tr>
<tr>
<td>FoM [dBc/Hz]</td>
<td>196</td>
<td>193</td>
<td>190</td>
</tr>
<tr>
<td>Topology</td>
<td>Class-C (single)</td>
<td>Transformer feedback</td>
<td>Class-C (dual)</td>
</tr>
</tbody>
</table>

Conclusion

- A 0.2V LC-VCO is realized by using a dual-conduction Class-C topology, which has a smaller conduction angle than the conventional Class-C VCO under the low supply voltage condition.
- The significance of this work is improvement of FoM for the low-voltage oscillators.
- A low-jitter and low-power clock generator can be realized.
- Bias generation is a remaining issue.