Passive Device Characterization for 60-GHz CMOS Power Amplifiers

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Motivation

60GHz unlicensed band

- 9GHz-BW around 60GHz
  - Several-Gbps wireless communication
- Use of CMOS process
  - Fab. cost is very important to generalize it. RF&BB mixed chip can be realized.

Our target

60GHz 2.16GHz-full 4ch direct-conversion by CMOS Tr
QPSK 3Gbps & 16QAM 6Gbps & 64QAM 9Gbps
IEEE 802.15.3c conformance
Dynamic power management: <300mW for RF front-end
Circuit blocks of 60GHz transceiver

60GHz LNA

Down-Mixer

20GHz PLL

Up-Mixer

60GHz PA

60GHz Tripler with quadrature output
Matching is very important for mmw circuit design, because:

1. The wave length is very short,
2. Tr’s gain is very small, and
3. Loss of TL is very large.

At 60GHz, every interconnects should be dealt with as a distributed component.

The accurate characterization is required.
Overview of device characterization

Initial T.O. for **Modeling**
- Transistors (CS, CG with various layouts)
- Transmission line (various length & $Z_0$)
- Branch & bend line
- Spiral inductor
- Balun
- Series capacitor
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier for the model evaluation
- DC probe

Second T.O.
- Circuit building blocks
- Whole system
Overview of characterization

• Transmission line
• Branch & bend line
• Decoupling capacitor
• De-embedding patterns
• 1-stage amplifier
• DC probe
• 4-stage power amplifier
Dummy metal

To avoid random production of dummy metal, it is manually placed to keep good reproducibility.
Tile-base layout

Each component is previously measured and modeled. The same layout is utilized to maintain modeling accuracy.
Transmission line in CMOS chip

Guided microstrip line

\[ e^{-\gamma \ell} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \]

\[ K = \left\{ \frac{(S_{11}^2 + S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{\frac{1}{2}} \]

\[ Z^2 = Z_0^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} \]

\[ \gamma = \alpha + j \beta \]

Slow-wave coplanar-waveguide is also utilized depending on a required characteristic impedance.
Cross-sectional structure

3.5Ω/mm

Top metal

1.2um

8.0um

Metal 1 (shield/slit)

0.2um

0.3um

Substrate

320um
To meet measured $\alpha$, $\beta$, $Q$ and $Z_0$, substrate model is individually extracted for each structure.
Improved Mangan’s method is utilized with 200µm and 400µm transmission lines.

Transmission line (400µm)

400µm of transmission line has almost the same characteristics with that of 200µm, which is a good proof of accurate modeling.
Overview of characterization

• Transmission line
• Branch & bend line
• Decoupling capacitor
• De-embedding patterns
• 1-stage amplifier
• DC probe
• 4-stage power amplifier
Branch & bend modeling

With 200µm shunt TL

With 300µm shunt TL

Each red-box part is characterized as a combination of optimized transmission lines.
T-junction modeling

Lower $Z_0$ TLs are utilized, and $Z_0$ is adjusted for the measurement results.

**Dummy metal causes unexpected response.**
Experimental results for T-junction

T-junction with 200µm shunt TL

T-junction with 300µm shunt TL

No model

ADS model

Our model

Our model extracted from 200µm TEG

S(2,1) [dB]

Measurement
Without T model
With T model
Modeling

Frequency [GHz]

0 20 40 60

0 20 40 60

S(2,1) [dB]

Measurement
Modeling
Overview of characterization

- Transmission line
- Branch & bend line
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier
- DC probe
- 4-stage power amplifier
MIM capacitor for de-coupling

Area efficiency is large, but the self-resonance freq. is low.

The regular layout of MIM cap. cannot be used at 60GHz.
Interdigital MIM capacitor

Interdigital structure with the optimized finger length is utilized.

MIM cap. is modeled as a low-impedance transmission line.

↑ to DC-Pad

↓ to Matching block
Distributed modeling of MIM cap.

Modeled as a transmission line

reflection 1-67GHz
Overview of characterization

• Transmission line
• Branch & bend line
• Decoupling capacitor
• De-embedding patterns
• 1-stage amplifier
• DC probe
• 4-stage power amplifier
An evaluation using a 1-stage amplifier

Comparison between model and measurement.
Model evaluation in input & output reflection

S\textsubscript{11}(gate-side reflection)  S\textsubscript{22}(drain-side reflection)

De-coupling MIM model is required for reliable design. 90nm CMOS is used.
Other modeling issues

• De-embedding
• Transistor layout optimization
• Spiral inductor
• Balun
• RF Pad
• DC probe / bonding wire / bump / filler / PCB
Each component is implemented as an in-house PDK for Agilent ADS.
Overview of characterization

• Transmission line
• Branch & bend line
• Decoupling capacitor
• De-embedding patterns
• 1-stage amplifier
• DC probe
• 4-stage power amplifier
4-stage class-A Power Amplifier

- CMOS 65nm process
- Short stub

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Chip micrograph

60GHz CMOS PA

0.85mm

OUT

1.5mm

surface ground plane

CMOS 65nm process

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Measurement results

@61.5GHz
S_{21}: 16.4\,\text{dB}
S_{11}: <-8\,\text{dB}
S_{22}: <-10\,\text{dB}
Measurement results

*Power gain*: 16.4dB  
*P*$_{1\text{dB}}$: 4.6dBm  
*P*$_{\text{DC}}$: 122mW
# Measurement summary

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<th>Reference</th>
<th>Technology</th>
<th>Freq. [GHz]</th>
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In this presentation, I presented a modeling approach to design a 60GHz CMOS amplifiers.

1. Design issue of TL on CMOS chips is different from that of compound semiconductors. e.g., dummy metal, lossy substrate, large conductive loss, etc
2. Branch modeling
3. Distributed modeling of de-couple MIM cap.
4. Evaluation using a 1-stage amplifier

By the proposed modeling method, 60GHz power amplifier can be successfully realized.
Acknowledgement

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