A 0.9-3.0 GHz Fully Integrated CMOS Power Amplifier for Multi-Band Transmitters

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Outline

• Introduction
• PA design
• Measurement results
• Conclusion
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Single chip transceiver

• Conventionally, PA is fabricated in compound semiconductor such as GaAs

• Recently, CMOS PA is under hot debate to realize single chip transceiver
The target of this work is to cover multiple wireless standards with only one CMOS PA
Isolator-less transmitter

- Function of isolators
  - Maintain PA’s output impedance 50Ω
  - Protect PAs from reflected wave

Isolators can be removed if PAs have 50Ω output impedance

- Conventional
- Proposed

Reducing off-chip component
Challenges of CMOS PA

- Low breakdown voltage of transistor
  - In submicron CMOS process, $V_{DD}=1\sim2\text{V}$
  - Output power $\propto (\text{Voltage})^2$
  - 10V amplitude for 1W output power

Solution

- Use thick-oxide transistor
- Apply cascode topology and share output voltage
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Conventional approach

Distributed amplifier

✓ Wideband input and output matching
✗ Large chip area
✗ Small output power due to the absence of impedance transformation
Output impedance tuning 1

If \( r_{ds} = \infty \),

\[
Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{1}{j\omega C} \parallel (R_L + j\omega L)
\]

When \( f = \frac{1}{2\pi \sqrt{LC}} \) (Resonance frequency)

\[
Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{L}{CR_L}
\]

Tune C to cancel imaginary part of \( Z_{out} \) at arbitrary frequency

\( R_s \) : source impedance (50\(\Omega\))

\( R_L \) : inductor parasitic resistance
Output impedance tuning 2

\[ Z_{\text{out}} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{L}{CR_L} \]

- Tune \( R_f \) to match \( Z_{\text{out}} \) to 50\( \Omega \)
- Since \( Z_{\text{out}} \) depends on the value of \( C \), \( R_f \) needs to be changed according to the matching frequency

In fact, \( r_{ds} \) is small... \( \Rightarrow \) Cascode topology is used

\( R_s \) : source impedance (50\( \Omega \))
\( R_L \) : inductor parasitic resistance
Schematic of the proposed PA

- Variable capacitance
- Variable resistance
- Parallel resonance
- Change output matching band by switching C and R
- Differential topology for 3dB larger $P_{\text{sat}}$
- Class-A bias
State of switches

Frequency

0.9 GHz 3.0 GHz

Band 1
- 4.8 pF
- 2.4 pF
- 1.9 pF

Band 2

Band 3

Band 4

0.8 kΩ 1.1 kΩ 1.6 kΩ
Theoretical maximum output power

- **Without impedance transformation**

\[ P_{\text{sat}} = \frac{(6.6V)^2}{2 \cdot 100\Omega} = 0.22\text{W (23dBm)} \]

- **With impedance transformation**

\[ P_{\text{sat}} = \frac{(3.3V)^2}{2 \cdot 10\Omega} = 0.54\text{W (27dBm)} \]

- Impedance transformation network can enhance the output power, but it is usually narrow-band

- 23dBm \( P_{\text{sat}} \) can be achieved due to differential topology and high \( V_{\text{DD}} \)
Voltage stress of switches

- Maximum voltage swing at output node is about $V_{DD}=3.3V$
- The same voltage is applied to switches when they are off

Thick oxide nMOS is applied as switch
Switch biasing

- Large voltage swing makes off-state switch on for a moment
- Degrade large signal characteristics such as $P_{1dB}$

Bias to source and drain of off-state switches

Diagram showing voltage components $V_x$, $V_{DD}$, $V_{th}$ with and without bias.
Simulation of switch biasing effect

- $P_{1dB} = 22\, \text{dBm}$
- $P_{1dB} = 13\, \text{dBm}$

Off-state switches start to be on
Chip micrograph

- 0.18µm CMOS
- Chip was measured using probes and external DC block capacitors
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Small signal S-parameters

- Differential-mode S-parameter calculated from 4-port S-parameter

Solid line : Simulation
Marker : Measurement

0.9~3.0GHz, $S_{22} < -10\text{dB}$, $S_{21} > 16\text{dB}$
Large signal measurement setup

Input loss

Output loss

• Input and output losses are calibrated from results
Large signal measurement result

@2.4GHz, Band4

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{1dB}$</td>
<td>18.6dBm</td>
</tr>
<tr>
<td>$P_{sat}$</td>
<td>21.7dBm</td>
</tr>
<tr>
<td>PAE$_{max}$</td>
<td>22.6%</td>
</tr>
</tbody>
</table>
• Measured large signal performance in each band and each signal frequency

• $P_{sat}$ is larger than 19dBm, and $PAE@peak$ is larger than 11% at the entire frequency range
## Comparison of CMOS PAs

<table>
<thead>
<tr>
<th></th>
<th>Technology</th>
<th>$V_{DD}$ [V]</th>
<th>Frequency [GHz]</th>
<th>$P_{sat}$ [dBm]</th>
<th>PAE@peak [%]</th>
<th>Area [mm$^2$]</th>
<th>Output matching</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFIC ’04 [4]</td>
<td>0.13$\mu$m CMOS</td>
<td>2.0</td>
<td>2.0 ~ 8.0</td>
<td>7 ~ 10</td>
<td>2 (@1dB)</td>
<td>—</td>
<td>Wideband</td>
</tr>
<tr>
<td>ISSCC ’09 [5]</td>
<td>0.13$\mu$m CMOS</td>
<td>1.5</td>
<td>0.5 ~ 5.0</td>
<td>14 ~ 21</td>
<td>3 ~ 16</td>
<td>3.6</td>
<td>Wideband</td>
</tr>
<tr>
<td>T-MTT ’07 [6]</td>
<td>0.18$\mu$m CMOS</td>
<td>2.8</td>
<td>3.7 ~ 8.8</td>
<td>16 ~ 19</td>
<td>8 ~ 25</td>
<td>2.8</td>
<td>Wideband</td>
</tr>
<tr>
<td>ISSCC ’09 [7]</td>
<td>0.13$\mu$m CMOS</td>
<td>3.0</td>
<td>1.0 ~ 2.5</td>
<td>28 ~ 31</td>
<td>18 ~ 43</td>
<td>2.56*</td>
<td>Wideband</td>
</tr>
<tr>
<td>This work</td>
<td>0.18$\mu$m CMOS</td>
<td>3.3</td>
<td>0.9 ~ 3.0</td>
<td>20 ~ 22</td>
<td>11~ 23</td>
<td>1.03</td>
<td>Tunable</td>
</tr>
</tbody>
</table>

*With distributor
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Conclusion

• Output impedance tuning method utilizing LC-resonance and resistive feedback is proposed
• 0.18µm fully integrated CMOS PA
• 0.9-3.0 GHz output matching
• At the entire frequency range, over 19dBm output power and over 11% PAE is achieved
Thank you for your attention!