Technology Trend of ADCs

Akira Matsuzawa

Department of Physical Electronics
Tokyo Institute of Technology

2008.10.31

A. Matsuzawa
Contents

- Issues of pipeline ADCs
- Revolution of SA ADCs
- Fight back of pipelined ADCs
- What determines FoM
- Summary
Mega-technology trend in ADCs

A major conversion scheme of ADCs is now changing from pipeline to SA

Pipeline ADC

Opamp-base design
Opamp determines performance
Static current flows

SA: Successive Approximation

Comparator-base design
Comparator determines performance
No static current flows

SA ADC

2008.10.31 A. Matsuzawa
Issues of pipeline ADCs
(current major ADC architecture)
Folding I/O characteristics makes higher resolution along with pipeline stages.
Issues of pipeline ADCs

Major issues of pipeline ADCs are caused by OpAmp. Scaled CMOS (90nm) can’t realize high OPamp Gain.

\[ G_{DC} (dB) > 6N + 10 \]

10b : 70dB
12b : 82dB

Sub-100nm CMOS
\[ G_{DC} \approx \left( \frac{V_A}{V_{eff}} \right)^n \approx \left( \frac{1}{0.15} \right)^n \approx 16dB \times n \]
\[ n < 5 \]
\[ G_{DC} < 80dB \]
Conversion speed of pipeline ADC

Speed of pipeline ADC is proportional to the OPamp current basically.

\[ f_c \approx \frac{3 \times \text{GBW}_{\text{close}}}{N} \propto \frac{I_{ds} \beta(I_{ds})}{C_L(I_{ds})} \]

\[ \text{GBW}_{\text{close}} = \frac{g_m \cdot \beta}{2 \times C_L} = \frac{g_m}{2 \times C_o} \left( \frac{2 + C_{pi}}{C_o} \right) \left( 1 + \frac{C_{po}}{C_o} \right) + \left( 1 + \frac{C_{pi}}{C_o} \right) \]

\[ = \frac{I_{ds}}{C_o V_{eff}} \left( 2 + \frac{\alpha_{pi} I_{ds}}{C_o} \right) \left( 1 + \frac{\alpha_{po} I_{ds}}{C_o} \right) + \left( 1 + \frac{\alpha_{pi} I_{ds}}{C_o} \right) \]

Performance model


\[ g_m = \frac{2 I_{ds}}{V_{eff}} \]

\[ C_{pi} = \alpha_{pi} I_{ds}, \quad C_{po} = \alpha_{po} I_{ds} \]

\[ \alpha_{pi}, \alpha_{po} \text{ are design rule dependent} \]
Capacitances: Signal and parasitic

Parasitic capacitance can be reduced by technology scaling, however, capacitance for signal will increase.

\[ C_o \geq 1.66 \times 10^{-19} \left( \frac{2^N}{V_{sig}} \right)^2 \]

\[ V_{sig} = 2(V_{dd} - 4V_{eff}) \]

\[ V_{eff} = 0.15V \]

\[ C_o \propto \left( \frac{2^N}{V_{sig}} \right)^2 \]

\[ C_p \propto \frac{1}{S^2} \]

Required capacitance for signal

Parasitic capacitance

For signal

Parasitic
Performance summary

Scaled CMOS is effective for just low resolution ADC.
Scaled CMOS is not effective for high resolution ADC.
Speed and power

Conversion speed has saturated at 200 MHz
Lower mW/MHz is needed for low power operation.
Revolution of SA ADCs

(Low FoM ADC architecture)
SA ADC

Successive Approximation ADC is free from OpAmp design issues and looks suitable for sub-100nm CMOS era.

Require only capacitors, switches, comparator, and logics.

No quiescent current → extremely low power

Binary search algorithm

Binary weighted Capacitor array

Comparator
Performance overview of SA ADCs

SA ADCs become dominant in every performance range. In particular FoM has rapidly lowered.

1/200 during past three years.

Courtesy Y. Kuramochi
SA ADC: The most simplest ADC

The most simplest ADC architecture:
No static current and the passives determine the SA ADC performance.
In contrast, OPamp determines the performance of pipeline ADC.

Sample and hold

Quantization
Comparing between reference voltage and signal

\[ n C_s (V_o - V_{ref}) + (1 - n) C_s V_o = -Q_s \]
\[ \therefore n C_s V_{ref} - C_s V_o = Q_s = C_s V_{sig} \]
\[ \therefore V_o = -\left( V_{sig} - n V_{ref} \right) \]
SA ADC must be the best solution for scaled analog technology. No OpAmp is needed.

No static power consumption.
Higher signal swing and small capacitance

\[ Q_{\text{REF}} = \sum_{i} 2^{i} C_{U} \cdot V_{DD} \]

Analog operation with capacitances

Capacitances can realize analog operation for SAR ADC. No static current is required and higher signal swing can be used.

\[ Q = \frac{C_S}{2} \times V_{IN} - 128 \times C_U \times V_{DD} + 64 \times C_U \times V_{DD} \pm \ldots \]
Results

Amazing small FoM=65fJ/step has been attained.

8bit, 0.3mW at 20MHz

J. Craninckx and G. Van der Plas,
“A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS,”

<table>
<thead>
<tr>
<th>ISSCC06 Paper #</th>
<th>Arch.</th>
<th>Fs [MS/s]</th>
<th>ENOB</th>
<th>P [mW]</th>
<th>FoM [fJ]</th>
<th>FoM includes</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>CTΔΣ</td>
<td>40</td>
<td>12</td>
<td>50</td>
<td>300</td>
<td>Ref. Yes</td>
</tr>
<tr>
<td>3.4</td>
<td>ΔΣ</td>
<td>4.4</td>
<td>12.6</td>
<td>13.8</td>
<td>500</td>
<td>Clock No</td>
</tr>
<tr>
<td>12.1</td>
<td>PL</td>
<td>100</td>
<td>9.4</td>
<td>39</td>
<td>570</td>
<td>Dec. No</td>
</tr>
<tr>
<td>12.3</td>
<td>Subr.</td>
<td>50</td>
<td>10.4</td>
<td>30</td>
<td>440</td>
<td></td>
</tr>
<tr>
<td>12.4</td>
<td>PL-CBSC</td>
<td>7.9</td>
<td>8.7</td>
<td>2.5</td>
<td>760</td>
<td></td>
</tr>
<tr>
<td>12.5</td>
<td>SAR</td>
<td>0.1</td>
<td>10.5</td>
<td>0.025</td>
<td>170</td>
<td></td>
</tr>
<tr>
<td>12.7</td>
<td>PL</td>
<td>50</td>
<td>9.2</td>
<td>15</td>
<td>510</td>
<td></td>
</tr>
<tr>
<td>31.1</td>
<td>Flash</td>
<td>1250</td>
<td>3.7</td>
<td>2.5</td>
<td>160</td>
<td></td>
</tr>
<tr>
<td>31.5</td>
<td>SAR</td>
<td>300</td>
<td>5.3</td>
<td>2.65</td>
<td>220</td>
<td></td>
</tr>
<tr>
<td>This work</td>
<td>CS-SAR</td>
<td>20</td>
<td>7.8</td>
<td>0.29</td>
<td>65</td>
<td></td>
</tr>
</tbody>
</table>
World lowest FoM ADC

Extremely low FoM of 4.4fJ/conv-step. SA ADC has been realized


Multi-step charging can reduce energy more

\[ E_{\text{diss}} = n \cdot \frac{1}{2} \cdot C_{\text{eq}} \cdot \left( \frac{V_b}{n} \right)^2 = \frac{1}{n \cdot 2} \cdot C_{\text{eq}} \cdot V_b^2 \]

Simple SA architecture

Multi-step charging (Adiabatic charging)
Comparison with state-of-the-art ADCs

Low FoM <100fJ/conv.-step ADCs become major.

This work

ISSCC 2007

ISSCC 2008
Reduction of area of SA ADC

One issue of current SAR is not small occupied area. This is due to large capacitance ratio; $C_{\text{MSB}}/C_{\text{LSB}}=2^N$. Serial capacitors can reduce this ratio, however parasitic capacitors degrade accuracy. We solved it by calibration.

Yasuhide Kuramochi, Akira Matsuzawa, and Masayuki Kawabata

"A 0.05-mm$^2$ 110-uW 10-b Self-Calibrating Successive Approximation ADC Core in 0.18-um CMOS"
Effect of digital calibration

We can realize 10b ADC with high SFDR of 72dB ADC in world smallest chip size, by using digital calibration technique.

Fight back of pipeline ADCs
Optimization of OpAmp in Pipelined ADC

90nm CMOS, near sub-threshold operation, and SC level-shift have realized 10bit 80MHz ADC with 0.8V operation and small power of 6.5mW

M. Yoshioka, M. Kudo, T. Mori, and S. Tsukamoto
“A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing,” ISSCC, Dig. Tech. paper, pp. 452-453, 2007.
Results

Excellent FoM has been attained in spite of pipeline ADC.

FoM=200fJ/step 0.08mW/MHz

<table>
<thead>
<tr>
<th>Technology</th>
<th>1P10M 90nm CMOS with MIM Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10bit</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>80MS/s</td>
</tr>
<tr>
<td>Active Area</td>
<td>1.18mm x 0.54mm</td>
</tr>
<tr>
<td>Input Range</td>
<td>1.2Vp-p Differential</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>0.8V &amp; 1.2V</td>
</tr>
<tr>
<td>SNDR</td>
<td>55.0dB @2MHz 51.4dB @41MHz</td>
</tr>
<tr>
<td>Total Power Consumption</td>
<td>6.5mW &amp; 13.3mW</td>
</tr>
<tr>
<td>SNDR @ Supply Voltage</td>
<td>56.9dB @2MHz 55.6dB @41MHz</td>
</tr>
<tr>
<td>INL</td>
<td>&lt; 1.0LSB &amp; &lt; 0.5LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>&lt; 0.8LSB &amp; &lt; 0.4LSB</td>
</tr>
</tbody>
</table>

Fclk=80MS/s, Fin=11MHz

Supply Voltage [V]
Optimization of $V_{\text{eff}}$

Optimum $V_{\text{eff}}$ is a function of resolution, current, and design rule. The lower $V_{\text{eff}}$ is recommended for scaled CMOS technology.

Process improvement of MOS transistor

No pocket transistor with low threshold voltage transistor offers low on-resistance for switches


Lmin (HPA)=0.14µm

Ron versus input (Vin)

Vt versus length (L)
Optimization of MOS transistor

No-pocket MOS transistor can increase output resistance and results in increasing the DC gain.
Summary of performance

This pipeline ADC has attained excellent low FoM compatible with SA ADC

<table>
<thead>
<tr>
<th>Resolution</th>
<th>10 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling speed</td>
<td>100MS/s</td>
</tr>
<tr>
<td>Input range</td>
<td>1.0Vppd</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>4.5mW</td>
</tr>
<tr>
<td>SNDR</td>
<td>59dB</td>
</tr>
<tr>
<td>DNL</td>
<td>+/-0.1 LSB</td>
</tr>
<tr>
<td>INL</td>
<td>+/-0.2 LSB</td>
</tr>
<tr>
<td>Active area</td>
<td>0.07mm^2</td>
</tr>
<tr>
<td>Technology</td>
<td>ST CMOS 65nm</td>
</tr>
</tbody>
</table>

FoM = 62fJ/conv.-step

<table>
<thead>
<tr>
<th>Tech (nm)</th>
<th>VDD (V)</th>
<th>Fs (MHz)</th>
<th>Power (mW)</th>
<th>SNDR (dB)</th>
<th>FOM (pj/step)</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>130</td>
<td>1.2</td>
<td>120</td>
<td>90</td>
<td>57.1</td>
<td>1.25</td>
<td>B.Hemes ISSCC-2004</td>
</tr>
<tr>
<td>90</td>
<td>1.2</td>
<td>12</td>
<td>3.3</td>
<td>52.6</td>
<td>0.76</td>
<td>R.Wang ISSCC-2005</td>
</tr>
<tr>
<td>90</td>
<td>1.2</td>
<td>100</td>
<td>35</td>
<td>56.9</td>
<td>0.6</td>
<td>G.Geelen ISSCC-2006</td>
</tr>
<tr>
<td>90</td>
<td>1.0</td>
<td>100</td>
<td>33</td>
<td>55.3</td>
<td>0.69</td>
<td>K.Honda JSSCC-2007</td>
</tr>
<tr>
<td>90</td>
<td>0.8</td>
<td>80</td>
<td>6.5</td>
<td>55</td>
<td>0.17</td>
<td>M.Yoshioka ISSCC-2007</td>
</tr>
<tr>
<td>65</td>
<td>1.2</td>
<td>100</td>
<td>4.5</td>
<td>59</td>
<td>0.062</td>
<td>This work</td>
</tr>
</tbody>
</table>

2008.10.31
A. Matsuzawa
Our original work

What determines FoM

OpAmp based design vs. comparator based design
OpAmp based vs. comparator based

Pipelined ADC

Opamp base

SA ADC

Comparator base
Noise of OpAmp

Amplification phase

\[ v_{no}^2 = \int_0^\infty \frac{i_n^2}{(g_m\beta)^2 + (\omega C_L)^2} \, df = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C_f} \]

\[ v_{no}^2 = \frac{\gamma \cdot n \cdot kT}{\beta C_L} + \frac{kT}{C_f} \quad C_i = C_s = C_o \]

\[ n=2: \text{Cascode} \quad n=3: \text{Folded Cascode} \]

\[ v_{nl}^2 = \frac{kT}{C_o} + \sum_{i=1}^{N-1} \frac{1}{2^i} \cdot v_i^2 = \frac{kT}{C_o} + \sum_{i=1}^{N-1} \frac{2^i}{2^{2i}} \cdot v_i^2 \approx 2 \frac{kT}{C_o} + \frac{\gamma n kT}{\beta C_L} \]
FoM calculation

We can estimate FoM for pipeline ADC.

Noise $\rightarrow$ Capacitance, Freq $\rightarrow$ Current

\[
v_{nt}^2 = 2\frac{kT}{C_o} + \frac{\gamma nkT}{\beta C_L} \approx \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{C_o}
\]

\[
V_{qn}^2 = \frac{1}{3}\left(\frac{q}{2}\right)^2 = \frac{1}{3}\left(\frac{V_{dd} - 2V_{eff}}{2^N}\right)^2 \quad \text{if} \quad V_{nt}^2 = V_{qn}^2 \quad \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{C_o} < V_{qn}^2
\]

\[
C_o > \left(2 + \frac{\gamma n}{\beta}\right)\frac{kT}{V_{qn}^2}
\]

\[
f_{close} > \frac{Nf_c}{3} \quad \therefore \frac{g_m\beta}{2\pi C_L} > \frac{Nf_c}{3} \quad \therefore g_m > Nf_c \frac{2\pi}{3\beta} C_o \quad g_m \approx \frac{2I_{ds}}{V_{eff}} \quad I_{ds} > Nf_c \frac{2\pi V_{eff}}{3\beta} \frac{2}{C_o}
\]

\[
P_d \approx 2.5 \times (2 \times 2 \times I_{ds} \times V_{dd}) = 10I_{ds}V_{dd}
\]

\[
FoM = \frac{P_d}{f_c \times 2^{N-0.5}}
\]
We are reaching the theoretical limit of FoM.

Measured FoM = 62 fJ/conv., Estimate FoM = 24 fJ/conv. For 10b ADC

\[
\begin{align*}
V_{\text{dd}} &= 1.0\text{(V)} \\
V_{\text{eff}} &= 0.15\text{(V)} \\
kT &= 4.1 \times 10^{-21} \\
\gamma &= 2 \\
n &= 2 \\
\beta &= \frac{1}{3} \\
f_c &= 100\text{MHz}
\end{align*}
\]

Recent ADC

\[
\begin{align*}
V_{\text{dd}} &= 1.2\text{(V)} \\
V_{\text{pp}} &= 1.0\text{V} \\
f_c &= 100\text{MHz} \\
C_0 &= 0.4\text{pF} \\
P_d &= 4.5\text{mW} \\
\text{SNDR} &= 59\text{dB} \\
\text{FoM} &= 62\text{fJ}
\end{align*}
\]

\[
\begin{array}{|c|c|c|c|}
\hline
\text{Resolution} & 10 & 12 & 14 \\
\hline
C_0 (\text{pF}) & 0.37 & 6.0 & 95 \\
\hline
I_{\text{dd}} (\text{mA}) & 1.75 & 33.6 & 628 \\
\hline
P_d (\text{mW}) & 1.75 & 33.6 & 628 \\
\hline
\text{FoM (fJ)} & 24 & 116 & 542 \\
\hline
\end{array}
\]

SA ADC needs high speed switches, comparators, and logics.

\[ P_d \approx f_c (N + 2)E_b \]

\[ E_b : \text{Energy / conv} \]

\[ T_{bc} = \frac{1}{f_c} \approx (N + 2)T_{bc} \]

\[ T_{bc} : \text{Bit cycle time} \]

\[ T_{set} : \text{Switch settling time} \]

\[ T_{cmp} : \text{Comparator decision time} \]

\[ T_{dig} : \text{Logic delay time} \]
Progress of CMOS Comparator

Small size MOS can be used for small mismatch circuits owing to analog compensation, however static current flows.


Mismatch vs. gate size

\[ \Delta V_T (mV) \propto \frac{T_{ox}}{\sqrt{LW}} \]

Chopper comparator solved this problem

Dingwall, RCA, 1979

Trade off

Small area
Low power
High speed

Small mismatch
Comparators

Dynamic comparators are widely used for not only SA ADCs but also Flash ADCs.

Dynamic comparators use the fast voltage fall depended on input voltage difference.


Issue of comparator for SA ADCs

A comparator has noise and this results in conversion error.

Comparator noise and ENOB

Small comparator noise is required for SA ADC

\[ \sigma_V < 0.25 \text{LSB} : -1 \text{bit deg rade} \]

\[ \sigma_V < 0.15 \text{LSB} : -0.5 \text{bit deg rade} \]

Analysis of comparator noise

Noise of dynamic comparator is mainly determined by internal capacitance. Thus low noise comparator consumes dynamic power.

Our original work

\[
\delta V_{in}^2 = \frac{4kT V_{dd}^2}{C_L V_{dd}^2} \left( \gamma \frac{V_{dd}}{V_{eff}} + 1 \right)
\]

\[
\langle v_n^2 \rangle = \frac{kT}{C_L}, \delta_{td} = \frac{\langle v_n^2 \rangle}{2} = \frac{kTC_L}{I_{ds}^2}
\]

\[
\delta_{td} = \frac{1}{I_{ds}} \left( \int_0^t n_i dt \right)^2
\]

\[
\delta_t = \frac{t_d}{2I_{ds}^2 S_{in}} = \frac{2kT \gamma t_d}{I_{ds} V_{eff}} = \frac{kT \gamma C_L V_{dd}}{I_{ds}^2 V_{eff}}
\]

\[
\delta_{td} = \frac{kT \gamma C_L V_{dd}}{I_{ds} V_{eff}} + \frac{kTC_L}{I_{ds}^2} \left( \gamma \frac{V_{dd}}{V_{eff}} + 1 \right)
\]

\[
\delta V_{in}^2 = \left( \frac{V_{eff}}{t_d} \right)^2 \frac{\Delta t_d}{t_d} = \left( \frac{V_{eff}}{t_d} \right)^2 \frac{V_{eff}}{t_d} \frac{kTC_L}{I_{ds}^2} \left( \gamma \frac{V_{dd}}{V_{eff}} + 1 \right)
\]

\[
= \frac{4kT V_{dd}^2}{C_L V_{dd}^2} \left( \gamma \frac{V_{dd}}{V_{eff}} + 1 \right)
\]
Sensitivity of comparator and FoM of ADC

The larger capacitance is required to realize higher resolution ADC. This results in increase of FoM.

\[ \delta V_{\text{in}} \propto \sqrt{\frac{1}{C_L}} \quad \text{FoM} \propto \frac{2(N + 2)C_L V_{dd}^2}{2^N} \]

\[ \delta V_{\text{in}}^2 = \frac{4kTV^2_{\text{eff}}}{C_L V_{dd}^2} \left( \frac{V_{dd}}{V_{\text{eff}}} + 1 \right) \]

\( V_{dd} = 1.0V, \ V_{\text{eff}} = 0.3V, \ \gamma = 1, \ T = 300K \)

Our original work

Sensitivity of comparator

\( V_{\text{in}} \) (mV) vs. \( C_L \) (fF)

FoM of ADC

SA ADC, N=10bit

\( V_{\text{in}} \) (mV) vs. \( C_L \) (fF)
Expected FoMs for comparators

FoM due to comparator in not negligibly small. Recent SA ADCs are reaching the limit. Measured FoM=4.4fJ/conv, Expected FoM is 1.4fJ/conv.

Our original work

\[ \delta V_{in}^2 = \frac{4kTV_{eff}^2}{C_L V_{dd}^2} \left( \gamma \frac{V_{dd}}{V_{eff}} + 1 \right) \]
\[ C_L > \frac{40kTV_{eff}^2 2^{2N}}{V_{dd}^4} \left( \gamma \frac{V_{dd}}{V_{eff}} + 1 \right) \]
\[ p_d = 2(N + 2)f_c C_L V_{dd}^2 \quad f_c=\text{100MS/s} \]
\[ \text{Resolution} \]

<table>
<thead>
<tr>
<th>FoM(fJ)</th>
<th>10</th>
<th>12</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL(fF)</td>
<td>42</td>
<td>670</td>
<td>11000</td>
</tr>
<tr>
<td>P_d(mW)</td>
<td>0.1</td>
<td>1.9</td>
<td>34</td>
</tr>
</tbody>
</table>

Comparison of FoM

FoM of SA ADC is one order of magnitude lower than that of pipeline ADC

### Pipeline ADC

<table>
<thead>
<tr>
<th>Resolution</th>
<th>10</th>
<th>12</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_o$ (pF)</td>
<td>0.37</td>
<td>6.0</td>
<td>95</td>
</tr>
<tr>
<td>$I_{dd}$ (mA)</td>
<td>1.75</td>
<td>33.6</td>
<td>628</td>
</tr>
<tr>
<td>$P_d$ (mW)</td>
<td>1.75</td>
<td>33.6</td>
<td>628</td>
</tr>
<tr>
<td>FoM (fJ)</td>
<td>24</td>
<td>116</td>
<td>542</td>
</tr>
</tbody>
</table>

**FoM=63fJ/Conv. step**


### SA ADC

<table>
<thead>
<tr>
<th>Resolution</th>
<th>10</th>
<th>12</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_L$ (fF)</td>
<td>42</td>
<td>670</td>
<td>11000</td>
</tr>
<tr>
<td>$P_d$ (mW)</td>
<td>0.1</td>
<td>1.9</td>
<td>34</td>
</tr>
<tr>
<td>FoM (fJ)</td>
<td><strong>1.4</strong></td>
<td><strong>6.5</strong></td>
<td><strong>30</strong></td>
</tr>
</tbody>
</table>

**FoM=4.4fJ/Conv. step**


---

2008.10.31

A. Matsuzawa
# Technology trend of ADCs

SA ADCs become major, but….

<table>
<thead>
<tr>
<th>Year</th>
<th>Description</th>
<th>Details</th>
<th>Notes</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008</td>
<td>Technology trend</td>
<td>Major in SA ADCs</td>
<td>Further developments</td>
<td>Reference 1</td>
</tr>
<tr>
<td>2010</td>
<td>Innovations</td>
<td>Continued improvements</td>
<td>Case studies</td>
<td>Reference 2</td>
</tr>
</tbody>
</table>

---

2008.10.31 A. Matsuzawa
Summary

• Pipelined ADCs, current major ADC architecture are now facing serious issues;
  – Need static current
  – Low OpAmp gain
  – Low voltage operation → larger capacitance
  – Scaled device is not suitable for higher resolution

• SA ADCs becomes attractive and looks suitable for scaled CMOS
  – Extremely small FoM
  – Simple, needs only capacitors, switches, comparators, and logics.
  – No static current
  – Free from OpAmp issues

• What determines FoM and which is better.
  – Pipeline: OpAmp    SA ADC: Comparator
  – SA is 10x better in FoM, however the difference is not so large.
  – FoM is reaching theoretical limit
  – Attention to the sensitivity of comparator for SA ADC design.