High speed ADCs: History and future

along with my life

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History of high speed ADCs along with my life
Start to develop ADCs

I joined Matsushita electric in 1978 after graduate from MS of Tohoku Univ. In 1979, I started to develop video-rate ADCs in Central research Lab.

In 1979, Panasonic released the monumental VTR that realized world first long play (2H → 6H) recording and became world top video supplier. $10B/year !!

This product must be the treasure of analog technology.

Panasonic =Matsushita Electric

1979, in front of Central research Lab.

Panasonic VHS Video NV-6000, 1979
Basic technologies for digital systems

At that time, Panasonic already started the development of digital video & TV systems.

Network, Communication
Storage media systems

Analog Processing  Data Converter  Communication processing  Data compression

- RF  - A/D Converter  - Mod/ Demod  - MPEG2, 4
- Optical I/F  - D/A Converter  - Channel select  - DSP
- Cable drive  - Signal Generation  - Error correction  - Codec
- Signal Generation  - Communication processing  - Protocol  - Codec

Analog technology  Digital technology

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NTU A. Matsuzawa
Video ADC board at 1980

A video rate ADC is the serious bottle neck for the digital consumer products.

My mission was to develop ADCs of which cost and power are low enough for consumer use.

10bit 14.3MHz ADC $10,000, Pd=20W !!

Analog Devices Inc.
I developed many ADCs to realize new digital consumer products.
Japan first video-rate 8b ADC

I succeeded to develop Japan first video-rate 8b ADC, in spite of my first work.

My first IC design At 1981

Bipolar (3um)
8b, 30MS/s, 0.7W
World first monolithic Video-rate 10b ADC

Only way to realize 10b video-rate ADC was to use high precision bipolar and array of comparators → Flash ADC

This ADC contributed to

Realization of world first HDTV
world first digital TV studio

Bipolar (3um)
10b, 20MS/s, 2W
$800


IR100 Award
Issue of flash ADC

Rapid increase of power dissipation $P_d, Area \propto 2^N$

Tough requirement for mismatch, 0.1mV $\Rightarrow$ Low yield

2mV : 10bit

Bip. Fast Bip. MOS

High precision bipolar

Ultra-fast bipolar

MOS device

Error 0.5 LSB below

Error 1.0 LSB below

Offset voltage fluctuation: $\sigma (\text{mV})$
10b, 20MHz, Bi-CMOS ADC for HDTV receivers

We developed ADC suitable for commercial HDTV receivers.

Two step parallel with interpolation

A. Matsuzawa ISSCC 1990.
Invention of the interpolation method

Compare interpolated amplified signals by resistor ladder

Philips group is another inventor

Remarkable invention award in 1994


Matsuzawa ISSCC 1990.
Effect of the interpolation method

Equivalent $V_q$ is $G$ times larger $\rightarrow$ relax mismatch

Effect of offset of amplifier to DNL can be reduced by $m$: # of interpolation

High production yield

Smooth conversion
Even if large offset

(a) A/D变换動作
(b) A/D变换特性

$\sigma_{off}^2 = \left( \frac{\sigma_{diff}}{m} \right)^2 + \left( \frac{\sigma_{comp}}{G} \right)^2$
Ultra-high speed ADCs have been developed.

8b, 120MHz, (1984)  M. Inoue and A. Matsuzawa, ISSCC 1984
World fastest 8b ADC

Contributed to the realization of HDTV camera and Digital oscilloscope

8b, 600MHz ADC (1991)  A. Matsuzawa, VLSI symposia 1991
World fastest 8b ADC

6b, 1GHz ADC (1991)  A. Matsuzawa, ISSCC 1991
World fastest in production
(Dual Parallel method)

Contributed to Digital oscilloscope
Digital Oscilloscope

Ultra-high speed ADCs realized Digital Oscilloscopes.

Yokogawa Electric  8b 1GHz (1994)
Ultra fast 10b 300MHz ADC

World fastest 10b ADC contributed to high speed optical communication for HDTV signals.

Bipolar 10b 300MHz, 4W

H. Kimura and A. Matsuzawa, VLSI Symposia '92
Interpolated parallel scheme

Relax mismatch $\rightarrow$ use of high speed transistors
High speed and high accuracy flash ADCs

Parallel

Interpolated parallel

Amplified signal is applied

Parallel Interpolated parallel

Amplified signal is applied
R&D 100 Award in 1994

Breakthrough in ultra fast signal processing

In Chicago
Digital Camera system

Digital camera system required ultra-low power ADCs

At that time, ADC consumed several 100 mW!!

@ 1988
Development of low power CMOS ADC and DAC

Digital handy VCR needs CMOS ADCs and DACs

1991

CMOS 8b ADC
CMOS 8b 3ch DAC
Early stage mixed signal CMOS LSI for CE

Success of CMOS ADC and DAC enabled low cost mixed signal CMOS LSI. This also enabled low cost and low power digital portable AV products.

1993 Model: Portable VCR with digital image stabilizing

Sub-ranging ADCs

Multi-step conversion can reduce the # of comparators. As a result, small power and area. However, it needs high precision comparators.

10bits: Flash; \(2^N - 1 = 1023\)

two step; \(2 \left(\frac{N}{2^2} - 1\right) = 62\)  

N. Fukushima, ISSCC 1989

Slide gauge

![Diagram of a sub-ranging ADC with inputs, comparators, and output stages.](image)
Chopper inverter comparator

CMOS has very large mismatch voltage and couldn’t be used in ADC.

Offset cancel and signal sampling with simple circuit
This invention opened the door of CMOS ADCs

Pros: Simple, low power, small area, low voltage, and sample and hold action
Cons: large absolute offset, suffer the power supply noise, sensitive to \( V_{dd} \).

A. Dingwall, JSC, SC-14, 1979

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A. Dingwall, JSC, SC-14, 1979
Two step parallel ADC

A two step parallel ADC needs signal sampling function. CMOS can realize it.

Realizing simultaneous signal sampling
2 channel lower conversion units realize two times higher operation
Overlap scheme relaxes needed offset voltage for comparators

N. Fukushima, ISSCC 1989
Ultra low power CMOS 10b ADC

To realize the digital handy video camera, Ultra low power ADC was needed.
We could develop world lowest power video-rate 10b, CMOS ADC.

CMOS 10b, 20MS/s, 30mW
K. Kusumoto, A. Matsuzawa
ISSCC '93, JSC 1993.

@0.8umCMOS ADC

Pd $\rightarrow$ 1/1000
Invention of capacitive interpolation

Simple circuits; switch, capacitors, and inverters
Amplify, offset cancel, interpolation, sampling

Relax mismatch
Reduce # of inverters

Removed inverter
Interpolation method

Interpolation can generate accurate intermediate references which are between two references. Thus step sizes are almost equal, even though mismatch voltages are large.

K. Kusumoto and A. Matsuzawa
Mixed signal tech. ; Digital read channel

Digital storage also needs high speed mixed signal technologies.

This system needs ultra-high speed and low power CMOS ADC

Data In (Erroneous)

Data Out (No error)

DVD, HDD

Variable Gain Amp. → Analog Filter → A to D Converter → Digital FIR Filter → Viterbi Error Correction

Voltage Controlled Oscillator

Clock Recovery

Analog circuit

Digital circuit

7b, 400MS/s
Progress in ultra-high speed ADCs

High speed ADCs have reduced power and area down to be embedded.

World fastest 6b ADC
6b, 1GHz ADC
2W,
1.5um Bipolar
A. Matsuzawa, SSCC 1991

World fastest CMOS ADC
6b, 800MHz ADC
400mW, 2mm²
0.25umCMOS

World lowest Pd HS ADC
7b, 400MHz ADC
50mW, 0.3mm²
0.18umCMOS

Reported Pd of CMOS ADCs

Conversion rate [x100Msps]
Pd/2^N[mW]

10mW/Gsps
1mW/Gsps

1 order down
This Work

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There are many types of comparator circuits, however all need static current.
A CMOS comparator is low power because of no need of static current.

Interpolation action

\[
\begin{align*}
G_1 &= K_p \left[ \frac{W_1}{L} (V_{in1+} - V_{th}) + \frac{W_2}{L} (V_{in2+} - V_{th}) \right] \\
G_2 &= K_p \left[ \frac{W_1}{L} (V_{in1-} - V_{th}) + \frac{W_2}{L} (V_{in2-} + V_{th}) \right]
\end{align*}
\]

If \( W_1 : W_2 = \frac{m-n}{m} : \frac{n}{m} \)

then, \((m-n)V_{in1+} + nV_{in2+} = (m-n)V_{in1-} + nV_{in2-}\)
Dynamic comparator

No static current and can realize interpolation without current consume, resistive interpolation.

Gate width ratio
\[ W1 : W2 = (m-n)/m : n/m \]
A 7b, 450MHz, 50mW CMOS ADC has been developed for the mixed signal SoC. This power dissipation is about 1/10, compared with the conventional high speed ADCs.


Technology: 0.18um CMOS(3AL,1PS)  
Area: 0.88mm X 0.34mm
Mixed signal SoC for DVD RAM system

Digital read channel can realize high readability for weak signal from DVD RAM pickup.

World fastest and highly integrated mixed signal CMOS SoC

S. Goto... A. Matsuzawa, ISSCC 2001.

0.18um- eDRAM

24M Tr
16Mb DRAM

500MHz
Mixed Signal
Full DVD system integration in 0.13um tech.

Advanced mixed signal SoC has been successfully developed.


0.13um, Cu 6Layer, 24MTr
Cost reduction in DVD Recorder

One-chip integration of hole DVD system has been realized. This makes circuit board simpler and contributes to the cost down, as well as performance up.

’2000 Model

’2003 Model
Power and area reduction of video-rate 10b ADCs have been reduced continuously. Currently, ADC can be embedded on a chip.
Power and area reduction of video-rate 10b ADCs

M. Hotta et al. IEICE 2006. June
Developed mixed signal CMOS LSIs

5G RF LAN
- 12b 50MHz ADC 2ch
- 12b 50MHz DAC 2ch

AFE for ADLS
- 12b 20MHz ADC+DAC

Digital network
- 1394b (1GHz)

AFE for Digital Camera
- 12b 20MHz ADC+AGC

2GHz RF CMOS
IEEE fellow

Elected IEEE fellow in 2002

for CONTRIBUTIONS to high-speed A/D converters and mixed-signal integrated circuits.