Numerical Analysis of Asymmetric Differential Inductors

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- Matrix-Decomposition Technique
- Simulation & Measurement Results
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Background

Miniaturization of CMOS process
- Difficulty of characterize on-chip inductors
- Degradation of circuit performances

- On-chip differential inductor
  Used for LC-VCO, differential LNA, Mixer…
  Mismatch between left and right halves degrades circuit performances.

Accurate modeling of on-chip symmetric inductor
- Extract of asymmetric parameters
Symmetric inductor analysis

• 3-port symmetric inductor analysis in various operation modes [1]
  - Circuit parameters are extracted by numerical optimization
  - Symmetry is assumed in the parameters
• Asymmetric properties are estimated from Y11 and Y22 [2]
  - The difference is involved in only difference in shunt parasitic components

\[
Z_{\text{diff}} = \frac{V_{\text{diff}}}{I_{\text{diff}}} = \frac{2(Y_{23} + Y_{13})}{Y_{23} (Y_{11} - Y_{12}) - Y_{13} (Y_{21} - Y_{22})}
\]

\[
L_{\text{diff}} = \frac{1}{\omega} \text{Im}(Z_{\text{diff}}) \quad Q_{\text{diff}} = \frac{\text{Im}(Z_{\text{diff}})}{\text{Re}(Z_{\text{diff}})}
\]

Proposed method
by Matrix-Decomposition Technique

Extract $\pi$-type equivalent circuit

- Physically reliable parameters can be extracted.
- The mismatch can be accurately evaluated.
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Overview

\[ Y_{\text{meas}} = Y_c + Y_{\text{sub}} \]

\[ Y_c: \text{Inductor core} \]

\[ Y_{\text{sub}}: \text{Interlayer-dielectric and Si substrate} \]

- All ports have common voltages
- \( Y_c \) can be ignored
- \( Y_{\text{sub}} \) is calculated from \( Y_{\text{meas}} \)
- \( Y_c \) is calculated from \( Y_{\text{meas}} \) and \( Y_{\text{sub}} \)
- \( Z_{\text{core}} \) is derived from \( Y_c \) by converting matrix

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Calculation of $Y_{\text{sub}}$

Voltages of each port are equal

- No current flows through $z_n$

\[
\begin{bmatrix}
i_1 \\
i_2 \\
i_3
\end{bmatrix} = Y_{\text{meas}} \begin{bmatrix} V_a \\ V_a \\ V_a \end{bmatrix}
\]

\[
= Y_c \begin{bmatrix} V_a \\ V_a \\ V_a \end{bmatrix} + Y_{\text{sub}} \begin{bmatrix} V_a \\ V_a \\ V_a \end{bmatrix}
\]

\[
= 0
\]

\[
Y_{\text{sub}} = \begin{bmatrix} y_{\text{sub}1} & 0 & 0 \\ 0 & y_{\text{sub}2} & 0 \\ 0 & 0 & y_{\text{sub}3} \end{bmatrix}
\]

\[
y_{\text{sub}1} = y_{\text{meas}11} + y_{\text{meas}12} + y_{\text{meas}13}
\]

\[
y_{\text{sub}2} = y_{\text{meas}21} + y_{\text{meas}22} + y_{\text{meas}23}
\]

\[
y_{\text{sub}3} = y_{\text{meas}31} + y_{\text{meas}32} + y_{\text{meas}33}
\]
Conversion of matrix $Y_c$ to $Z_{core}$

$Y_c = Y_{meas'} - Y_{sub}$

Define $Z_{core}$ by 2 $\times$ 2 matrix

$$Z_{core} = \begin{pmatrix} z_1 & -j\omega M_{12} \\ -j\omega M_{12} & z_2 \end{pmatrix}$$

$$v_z = Z_{core}i_z$$

$v_z = Av$  $i_z = Bi$

Obtain converting matrix $A$ and $B$

$B^T$ can be $A^*$  $AA^* = I$

e.g.) $v_z = \begin{pmatrix} v_{z1} \\ v_{z2} \end{pmatrix} = \begin{pmatrix} v_1 - v_3 \\ v_2 - v_3 \end{pmatrix}$  $i_z = \begin{pmatrix} i_{z1} \\ i_{z2} \end{pmatrix} = \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}$

$$A = \begin{pmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \end{pmatrix}$$  $$B = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}$$

Matrix $Y_c$ is converted into matrix $Z_{core}$

$$Av = Z_{core}Bi = Z_{core}BY_c v$$

$$A = Z_{core}BY_c$$

$$Z_{core} = (BY_cA^*)^{-1}$$
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Mismatch of ground loop

Flux loss: Only half side

Flux loss: Both sides

The inductance mismatch depends on the number of turns.

Odd ➔ Each loss is different ➔ Mismatch

Even ➔ Each loss is almost equal ➔ Mismatch
• Inductance mismatches are evaluated by the proposed method.
• The mismatches are plotted as a function of $\Delta x$. 
Simulation Result

- The mismatch of 2-turn is smaller than 1- and 3-turn.
- Increasing $\Delta x$, mismatch decreases.

![Graph showing simulation results](image)

- $L$ mismatch (%) vs. $\Delta x$ (µm) for 1-turn, 2-turn, and 3-turn.
Measurement

0.18 µm Si-CMOS
Line width: 9µm, Line space: 2µm
Inner diameter: 100µm, Turn: 3

Symmetric

Asymmetric

VNA: 4port 10MHz-67GHz
E8361A+N4421BH67 (Agilent)
Probe: I67-D-GSGSG-150 (Cascade)
I67-GSG-150 (Cascade)
Measurement Result

Symmetric

Mismatch 1.5%

Asymmetric

4.0%

• Influence of asymmetric ground loop is extracted
• Other reasons to cause asymmetry exist

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The numerical analysis using the matrix-decomposition technique is proposed

- Physically reliable parameter can be extracted
- The mismatch can be accurately evaluated

Proposed method is applied to 1-, 2-, and 3-turn differential inductors

Influence of asymmetric ground loop can be accurately extracted
Q factor

![Graphs showing Q factor for symmetric and asymmetric cases.](image)

**Symmetric**

**Asymmetric**
\begin{align*}
\mathbf{Z}_{\text{short}} \text{ and } \mathbf{Y}_{\text{open}} \text{ are removed by Open-Short de-embedding} \\
\mathbf{Z}_{\text{meas'}} &= (\mathbf{Y}_{\text{meas}} - \mathbf{Y}_{\text{open}})^{-1} - (\mathbf{Z}_{\text{short}} - \mathbf{Y}_{\text{open}})^{-1} \\
\mathbf{Y}_{\text{meas'}} &= \mathbf{Z}_{\text{meas'}}^{-1}
\end{align*}