Recent studies on the dynamic behavior of current-steering DACs

Matthias Frey and Akira Matsuzawa
Motivation, Background

- What is a current-steering DAC?

**ideal:**

- Load
  - \( V_0(t) \)
  - \( V_1(t) \)
- \( I_{b0} \)
- \( I_{b1} \)
- \( I_{bn} \)

**transistor-level:**

- \( R_{\text{Load}} \)
- \( V_0(t) \)
- \( V_1(t) \)
- \( V_{s0}(t) \)
- \( V_{s1}(t) \)
- \( V_x(t) \)
- \( V_{\text{bias}} \)
- \( V_{\text{casc}} \)

resistive load for current-to-voltage conversion

switches

scaled current sources

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Motivation

- Why should we care about dynamic properties?
  ...and not only about INL/ DNL?

SFDR vs. Signal Frequency

...later!

from:
Bugeja et al., “14-b, 100-MS/s CMOS DAC for spectral performance”, JSSC 1999

from:

from:
Q. Huang, “Low Voltage and Low Power Aspects of Data Converter Design”, ESSCC 2004
Motivation

- Switching in Current Steering DACs:

Ideally:

\[ V_0(t) \]

\[ V_1(t) \]

\[ V_{s0}(t) \]

\[ V_{s1}(t) \]

\[ V_{bias} \]

\[ V_{casc} \]

\[ I_{bias} \]
• Switching in Current Steering DACs:

![Diagram of Current Steering DACs](image)
Part I: Origin of reduced SFDR

- Switching Delay Differences:
  - Output-Dependent Delay Difference
  - Cell-Dependent Delay Difference

- Errors Introduced while Switching:
  - Switching Crossover
  - Charge Feed-through

- Resampling Circuits
  - Non-Return-to-Zero vs. Return-to-Zero
  - Dual Return-to-Zero Circuit
• **SFDR: Spurious Free Dynamic Range**

- many definitions of SFDR exist!
- many definitions of Spur exist, e.g., “non-harmonic”, “any non-signal component”
- various frequency bands of interest
- SFDR is generally a function of input-signal frequency and amplitude, and sampling frequency

Switching Delay Differences

• Cell-Dependent Delay Differences:
  – delay differences between current-sources is one of the main differences for bad SFDR.
  – delay determined by position of the current-cell in the layout
  – model discussed:
    • linearly-distributed delays are considered
    • maximum delay difference: $d_{\text{max}}$

discussed in:
T. Chen and G. Gielen,
Switching Delay Differences

- **Cell-Dependent Delay Differences:**
  
  **Main results:**
  
  - "worst case scenario":
    
    \[
    f_0 \leq \frac{2}{\pi d_{\text{max}} 10(6.02N+1.76)/20}
    \]
    
    e.g.: 10 bits DAC, \(d_{\text{max}} = 100\) ps
    
    \(\Rightarrow\) max. signal frequency: \(f_0 < 5\) MHz
    
  - The distribution of the delay values has the greatest impact on the SFDR, rather than the values itself.
    
    \(\Rightarrow\) switching sequence needs to be optimized

  discussed in:
  
  T. Chen and G. Gielen,
  
Switching Delay Differences

Cell-Dependent Delay Differences

Mathematical background

- Cell-Dependent Delay Differences
  - Switching Sequence
    - Optimal Switching Sequence
      - SFDR: DB
      - Signal Frequency: Hz

Fig. 4. Equation (37): the analysis and improvement of a current-steering DAC’s dynamic range-1: The cell-dependent delay differences, Jan. 2006.

⇒ switching sequence needs to be optimized


discussed in:
**Switching Delay Differences**

- **Output-Dependent Delay Differences:**
  - **Origin:**
    - A transistor switches at $V_{gs} = V_{th}$
    - Because of the Switch-transistor’s limited $(g_m \cdot r_0)$:
      \[
      V_x(t) = f(V_0(t), V_1(t), V_{s0}(t), V_{s1}(t))
      \]
    - $V_x(t) \approx V_0 / (1 + g_m r_0)$
  - $g_m, r_0$: transconductance and output resistance of the switch transistor

**Diagram:**

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"The analysis and improvement of a current-steering DAC’s dynamic range-II: The output-dependent delay differences", Feb. 2007.
Switching Delay Differences

• Output-Dependent Delay Differences:
  - As the clock-signals $V_{si}(t)$ have a finite slope and
  - the source voltage $V_x(t)$ depends on the output voltage, $V_i(t)$,
  $\Rightarrow$ the switch-delay depends on the output voltage.

$V_{s0}(t)$ $V_{s1}(t)$

$V_{bias}$ $V_{casc}$

$V_{x}(t)$

$V_{0}(t)$ $V_{1}(t)$ $V_{s0}(t)$ $V_{s1}(t)$

$R_{Load}$ $R_{Load}$

discussed in:
T. Chen and G. Gielen,
"The analysis and improvement of a current-steering DAC’s dynamic range-II: The output-dependent delay differences”, Feb. 2007.
Switching Delay Differences

Practical Example:

- max. output voltage swing: 0.5 V
- $g_m r_0 \approx 10$
- max. source voltage ($V_x$) variation: \( \approx 0.05 \) V
- rising speed of clock: 1.25 V/ns

\[ \text{\Rightarrow resulting delay difference: 40 ps} \]

```
V_{s0}(t)
```

```
V_{s1}(t)
```

```
t
```

```
\text{discussed in: T. Chen and G. Gielen,}
\text{"The analysis and improvement of a current-steering DAC's dynamic range-II:
The output-dependent delay differences"}, Feb. 2007.
```
Switching Delay Differences

- Output-Dependent Delay Differences:
  - Effects on the SFDR:

  \[
  \text{SFDR} = \frac{4}{\omega_0 d_{\text{max}}} \sqrt{\frac{1 + 4\omega_0^2 \tau^2}{1 + \omega_0^2 \tau^2}}
  \]

  \[
  \text{SFDR} \approx \frac{4}{\omega_0 d_{\text{max}}}
  \]

  SFDR decreases with:
  - increasing \( d_{\text{max}} \)
  - increasing signal frequency \( \omega_0 \)

  
  \[
  \text{SFDR} = \frac{32\tau}{\omega_0 d_{\text{max}}^2} \sqrt{\frac{1 + 9\omega_0^2 \tau^2}{1 + \omega_0^2 \tau^2}}
  \]

  \[
  \text{SFDR} \approx \frac{32\tau}{\omega_0 d_{\text{max}}^2}
  \]

  SFDR decreases with:
  - increasing \( d_{\text{max}} \)
  - increasing signal frequency \( \omega_0 \)
  - decreasing time constant \( \tau \)

  discussed in:
  T. Chen and G. Gielen,
  \textit{“The analysis and improvement of a current-steering DAC’s dynamic range-II: The output-dependent delay differences”}, Feb. 2007.
Switching Delay Differences

- Output-Dependent Delay Differences:
  - Effects on the SFDR:

single-ended output:  
\[
\text{Power} \quad | \quad 0 \quad 20 \quad 40 \quad 60 \quad 80
\]

\[
\text{Frequency [MHz]} \quad | \quad -200 \quad -150 \quad -100 \quad -50 \quad 0 \quad 50
\]

2nd-order harmonic

differential output:  
\[
\text{Power} \quad | \quad 0 \quad 20 \quad 40 \quad 60 \quad 80
\]

\[
\text{Frequency [MHz]} \quad | \quad -200 \quad -150 \quad -100 \quad -50 \quad 0 \quad 50
\]

3rd-order harmonic

discussed in:
T. Chen and G. Gielen,
Switching Delay Differences

• Output-Dependent Delay Differences:
  – Measures against it:
    • increase \((g_m \cdot r_0)\) of switches
      – add a cascode stage for switch
        (if voltage headroom permits)
      – scale the switches to increase \(g_m \cdot r_0\)
    • accelerate switching speed
    • add an RZ stage

discussed in:
T. Chen and G. Gielen,
Switching Current Sources

• Errors introduced while Switching:
  – “turning on”-transistor reaches different regions of operation at different times than its complementary “turning off” transistor.
  
  $V_{s1}(t)$
  $V_x(t)$
  $V_{s0}(t)$
  $V_0(t)$
  $V_1(t)$
  $V_{s1}(t)$
  $R_{Load}$
  $V_{bias}$
  $I_{bias}$
  $V_{casc}$
  $R_{Load}$

short time where both differential current-switches are off

→ abrupt discharge with steep transient

→ voltage $V_x$ drops

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Switching Current Sources

• Charge feed-through:
  – common problem for all SC- and SI-circuits
  – first order proportional to
    • switch-capacitance (switch-size)
    • switch-driving signal slope
    • switch-driving signal swing

– ideal switching scheme
  (for min. feed-through):
    • small switch
    • slow switch-driving signal
    • small switch-driving signal swing
Switching Current Sources

• How to improve switching behavior
  – ideal switching scheme:
  – for min. feed-through:
    • small switch
    • slow switch-driving signal
    • small switch-driving signal swing
  – for small output-dep. delay differences:
    • increase size of switches for large \((g_m \cdot r_0)\)
  – for short crossover time:
    • fast switching to minimize switching time
Switching Current Sources

• How to improve switching behavior
  – ideal switching scheme:
  – for min. feed-through:
    • small switch
    • slow switch-driving signal
    • small switch-driving signal swing
  – for small output-dep. delay differences:
    • increase size of switches for large $(g_m \cdot r_0)$
  – for short crossover time:
    • fast switching to minimize switching time

Switch Optimization:
• find ideal trade-off for switch-size
  (use cascode if head-room permits)
• slow switching signal, but with small signal-swing
NRZ vs. RZ, dual RZ:

- RZ, return-to-zero circuit:
  - each pulse returns to zero for a portion of the clock period

![Diagram showing conventional and return-to-zero DACs](image)

NRZ vs. RZ, dual RZ:

- RZ, return-to-zero circuit:
  - each pulse returns to zero for a portion of the clock period
  - solves inter-symbol interference problem
  - halves the output signal power, extra circuitry power
  - reduces SFDR for low frequency input signals
NRZ vs. RZ, dual RZ:

- RZ, return-to-zero circuit:
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from: Q. Huang, “Low Voltage and Low Power Aspects of Data Converter Design”, ESSCC 2004
NRZ vs. RZ, dual RZ

- **Dual RZ:**
  - RZ, return-to-zero circuit:
    - combines two shifted RZ-pulses to a single pulse

NRZ vs. RZ, dual RZ

• Dual RZ:
  – RZ, return-to-zero circuit:
    • combines two shifted RZ-pulses to a single pulse
    • solves inter-symbol interference problem
    • large circuit overhead
Part II: Modeling of DACs

- Simple Mathematical Model of a Current-Steering DAC’s Output
  - Code-Transition
  - Output-Dependent Delay Difference
  - The Simulink Model

- Future Work
  - Check whether the Model is precise enough
  - Build a Feedback Loop to Correct Non-Idealities
Preliminaries: Two Definitions

- **Glitch “Energy”, \( E_{\text{gl}} \):**
  - sometimes called “Glitch Area”
  - not an energy, but voltage integrated over time
  - Unit: often \([\text{pV} \cdot \text{s}]\)
  - many different definitions

- **Glitch Time, \( t_{\text{gl}} \):**
  - “time during which the glitch occurs”

\[
\begin{align*}
V_1(t) & \quad t_{\text{gl}}/2 \\
\end{align*}
\]
Simple Mathematical Model of a CS-DAC

• Current-Source Switching:
  – Code-Transition modeled by
    • shifted “tanh”-function
    +
    • exponentially-damped sinusoid as glitch

\[
i_{\text{out}} = A_{\text{gl}} \sin \left( \frac{2\pi}{T_{\text{gl}}} (t - t_0) \right) \exp \left( -\text{sign}(t - t_0) \frac{2\pi}{T_{\text{gl}}} (t - t_0) \right)
\]
\[
\quad + \frac{\text{level}_{i+1} - \text{level}_i}{2} \tanh \left( \frac{2\pi}{T_{\text{gl}}} (t - t_0) \right)
\]
\[
\quad + \frac{\text{level}_{i+1} + \text{level}_i}{2}
\]

discussed in:
J. Vandenbussche et al.,
Simple Mathematical Model of a CS-DAC

- Current-Source Switching:

\[
i_{\text{out}} = A_{\text{gl}} \sin \left( \frac{2\pi}{t_{\text{gl}}} (t - t_0) \right) \exp \left( -\text{sign}(t - t_0) \frac{2\pi}{t_{\text{gl}}} (t - t_0) \right) + \frac{\text{level}_{i+1} - \text{level}_i}{2} \tanh \left( \frac{2\pi}{t_{\text{gl}}} (t - t_0) \right) + \frac{\text{level}_{i+1} + \text{level}_i}{2}
\]

\[
E_{\text{gl}} = \frac{2R_{\text{load}}}{t_{\text{gl}}} \left( \frac{t_{\text{switched}}}{t_{\text{gl}}} \right) + \frac{1}{2} \frac{\text{level}_{i+1} - \text{level}_i}{2} \left( \tanh \left( \frac{2\pi}{5} \right) - 1 \right) \frac{t_{\text{gl}}}{4}
\]

- Parameters:

- Glitch Energy, \( E_{\text{gl}} \) → Glitch Amplitude \( A_{\text{gl}} \)
- Glitch Time, \( t_{\text{gl}} \)
- number of switches (involved in the code-transition)

discussed in:

J. Vandenbussche et al.,

Simple Mathematical Model of a CS-DAC

• From Transistor-Level to High-Level

1) Transistor-Level Simulation in Cadence:

2) Extract Parameters $E_{gl}$, $t_{gl}$

E$_{gl} = 8.9 \times 10^{-14}$ Vs
$t_{gl} \approx 0.5$ ps

3) High-Level Simulation with Extracted Parameters:

Input $E_{gl} = 1\times 10^{-13}$ V s, input $t_{gl} = 5\times 10^{-10}$ s
Simple Mathematical Model of a CS-DAC

- From Transistor-Level to High-Level
- Is the model precise enough?
  - Glitches are more symmetric in the mathematical model than in Cadence
  - With the same glitch-time, $t_{gl}$, the high-level simulation has a smaller bandwidth.
• From Transistor-Level to High-Level

• Is the model precise enough?
  
  – Glitches are more symmetric in the mathematical model than in Cadence
  
  – With the same glitch-time, $t_{gl}$, the high-level simulation has a smaller bandwidth.
Simple Mathematical Model of a CS-DAC

- **Output-Dependent Delay Difference**

\[
V_x(t) = \frac{V_0(t)}{1 + g_m r_0}
\]

\[
t_{\text{delay}} = \frac{t_{sw}}{V_{sw}(V_{th} + V_x(t))}
\]

\[
t_{\text{delay}} = \frac{t_{sw}}{V_{sw}(V_{th} + \frac{V_0(t)}{1 + g_m r_0})}
\]
Simulink Model of a CS-DAC

- Output of the Simulink Model:
Future Work

- Check if Model’s Precision is enough
- Design Feedback Loop to Correct Non-Idealities of DAC-Settling

(a) Feedforward with a separate calibration DAC.
(b) Feedback with a separate calibration DAC.
Conclusions

• The settling behavior of a current-steering DAC was discussed.

• Various reasons for SFDR degradation in current-steering DACs was presented.

• Hints for the design of the switches in current-steering DACs were given.

• A simple mathematical model of a current-steering DAC was presented.
Thank you for your interest!

for questions & comments:
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