Recent studies on the dynamic behavior of current-steering DACs

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In recent years, the interest in high-speed and high-resolution current-steering digital-to-analog converters (DACs) has greatly increased. Even though many medium-resolution DACs (of around 8–10 bits) for higher sampling frequencies exist, most of these DACs show poor performance for input signal frequencies approaching the Nyquist frequency [1], as can, e.g., be seen in Fig. 1. Therefore, it seems to be essential to study the dynamic behavior of DACs. It has been found that the cell-dependent delay differences [3], and the output-dependent delay differences [4] greatly limit the SFDR of high-speed DACs.

Our ongoing research focuses on building a high-level model of the DAC’s dynamic behavior and subsequently designing a digital calibration circuit that dynamically adjusts the input to the DAC to compensate for non-ideal dynamics.

References:

Fig. 1: SFDR versus input signal frequency, $f_{\text{amp}} = 100$ MHz (taken from [2]).