Trends in high speed ADC design

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  – Performance model of pipelined ADC

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  – Sub-ranging ADC
  – Successive approximation ADCs
  – Delta-sigma ADC
Speed and power

Conversion speed has saturated at 200 MHz. Smaller mW/MHz is needed for low power operation. 0.3mW/MHz for 10bit and 1mW/MHz for 12bit are the bottom lines.

**High Speed ADC**

**[Sampling Freq. VS Power]**

- 12Bit (Paper)
- 10Bit (Paper)
- 12Bit Products
- 10Bit Products.

JSSC, ISSCC, VLSI, CICC, ESSCC & Products

- 12b ≥ 10Bit, ≥ 1995-2006

- 10b

12bit : 1mW / MHz

10bit : 0.3 mW / MHz

ISSCC 2007

200MHz
Pipelined ADC

Folding I/O characteristics makes higher resolution along with pipeline stages.
Technology scaling can reduce parasitic capacitances. However signal capacitance will increase to keep the same SNR at lower voltage operation.

Parasitic capacitance → smaller
Operating voltage → lower
Signal swing → lower

Signal capacitance → larger
Voltage gain → lower

Technology scaling
We have developed the performance model for pipeline ADC that can treat technology scaling.

\[
\text{GBW}_{\text{close}} = \frac{g_m}{2\pi C_L} \beta
\]

\[
\beta = \frac{C_f}{C_f + C_s + C_{pi}}
\]

\[
C_L = C_{po} + C_{oL} + \frac{C_f (C_s + C_{pi})}{C_f + C_s + C_{pi}}
\]

\[
C_{oL} = \frac{C_s + C_f}{2}
\]

\[
C_o = C_s = C_f = C_{oL}
\]

\[
\text{g}_m : \text{Transconductance of input stage}
\]

\[
C_s, C_f : \text{Signal capacitance for feedback loop}
\]

\[
C_{pi}, C_{po} : \text{Input & output parasitic capacitance}
\]

\[
C_{oL} : \text{Load capacitance}
\]

\[
R_L : \text{Output resistance}
\]

\[
\omega_{p2} : \text{Second pole of OpAmp}
\]
Scaling and analog device and circuit parameters

Gate width and capacitances decrease with technology scaling.

\[
V_{\text{eff}} = 0.175 \text{V}
\]

\[
W = \frac{2L}{\mu C_{\text{ox}} V_{\text{eff}}^2} I_{\text{ds}}
\]

<table>
<thead>
<tr>
<th>DR</th>
<th>(W_N)</th>
<th>(W_P)</th>
<th>(V_{A,N})</th>
<th>(V_{A,P})</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>24.3</td>
<td>74.9</td>
<td>0.82</td>
<td>0.69</td>
</tr>
<tr>
<td>0.13 (\mu) m</td>
<td>37.5</td>
<td>147</td>
<td>0.82</td>
<td>0.64</td>
</tr>
<tr>
<td>0.18 (\mu) m</td>
<td>54.8</td>
<td>219</td>
<td>0.99</td>
<td>0.93</td>
</tr>
<tr>
<td>0.25 (\mu) m</td>
<td>116.0</td>
<td>396</td>
<td>0.78</td>
<td>0.97</td>
</tr>
<tr>
<td>0.35 (\mu) m</td>
<td>162.0</td>
<td>603</td>
<td>1.01</td>
<td>0.86</td>
</tr>
</tbody>
</table>

(b)\(C_{\text{pi},N}, C_{\text{pi},P}, C_{\text{po}}\) [fF/mA], \(\omega_{p2,N}, \omega_{p2,P}\) [GHz]

<table>
<thead>
<tr>
<th>DR</th>
<th>(C_{\text{pi},N})</th>
<th>(C_{\text{pi},P})</th>
<th>(C_{\text{po}})</th>
<th>(\omega_{p2,N})</th>
<th>(\omega_{p2,P})</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>23.7</td>
<td>93.4</td>
<td>94.5</td>
<td>9.35</td>
<td>15.4</td>
</tr>
<tr>
<td>0.13 (\mu) m</td>
<td>65.5</td>
<td>249</td>
<td>168</td>
<td>7.7</td>
<td>10.3</td>
</tr>
<tr>
<td>0.18 (\mu) m</td>
<td>115</td>
<td>475</td>
<td>340</td>
<td>2.06</td>
<td>4.7</td>
</tr>
<tr>
<td>0.25 (\mu) m</td>
<td>236</td>
<td>662</td>
<td>832</td>
<td>0.83</td>
<td>1.7</td>
</tr>
<tr>
<td>0.35 (\mu) m</td>
<td>303</td>
<td>1034</td>
<td>892</td>
<td>0.54</td>
<td>1.7</td>
</tr>
</tbody>
</table>
Determination of signal capacitance

Larger resolution requires larger signal capacitance. Furthermore, Voltage lowering increases signal capacitance more.

\[ C_o \geq 1.66 \times 10^{-19} \left( \frac{2^N}{V_{sig}} \right)^2 \]

<table>
<thead>
<tr>
<th>90nm</th>
<th>0.13 μm</th>
<th>0.18 μm</th>
<th>0.25 μm</th>
<th>0.35 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{dd} )</td>
<td>1.2V</td>
<td>1.5V</td>
<td>1.8V</td>
<td>2.5V</td>
</tr>
<tr>
<td>( V_{sig_{pp}} )</td>
<td>1.0V</td>
<td>1.6V</td>
<td>2.2V</td>
<td>3.6V</td>
</tr>
</tbody>
</table>

Gain Boost amp.

Output signal range \( V_{dd} - 4V_{eff} \)

\( 2V_{eff} \)

\( 2V_{eff} \)
Performance curve

Performance exhibits convex curve.
There is the peak conversion frequency and the optimum current.
Current increase results in increase of parasitic capacitances and decrease of conversion frequency in the higher current region.

\[
\text{GBW}_{\text{close}} = \frac{I_{ds}}{\pi C_o V_{\text{eff}}} \left( \frac{1}{2 + \frac{\alpha_{pi} I_{ds}}{C_o}} + \frac{\alpha_{po} I_{ds}}{C_o} \right) + \left( 1 + \frac{\alpha_{pi} I_{ds}}{C_o} \right)
\]

1. \(C_o \gg C_{po}, C_{pi}\)
2. \(C_{pi} < C_o < C_{po}\)
3. \(C_o < C_{po}, C_o < C_{pi}\)

\[
\text{GBW}_{\text{close}} \approx \frac{I_{ds}}{\pi C_o V_{\text{eff}}} \cdot \frac{1}{3} \quad (\propto I_{ds})
\]

\[
\text{GBW}_{\text{close}} \approx \frac{1}{\pi C_o V_{\text{eff}}} \cdot \frac{1}{3 + \alpha_o} \quad \text{(Constant)}
\]

\[
\text{GBW}_{\text{close}} \approx \frac{1}{\pi C_o V_{\text{eff}}} \cdot \frac{1}{3 + \alpha_i \alpha_o I_{ds}} \quad (\propto \frac{1}{I_{ds}})
\]
Performance summary

Scaled CMOS is effective for just low resolution ADC.
Scaled CMOS is not effective for high resolution ADC.
Optimization of OpAmp in Pipelined ADC

90nm CMOS, near sub-threshold operation, and SC level-shift have realized 10bit 80MHz ADC with 0.8V operation and small power of 6.5mW

M. Yoshioka, M. Kudo, T. Mori, and S. Tsukamoto
“A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing,” ISSCC, Dig. Tech. paper, pp. 452-453, 2007.
## Results

FoM=0.2pJ/step  0.08mW/MHz

<table>
<thead>
<tr>
<th>Technology</th>
<th>1P10M 90nm CMOS with MIM Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>10bit</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>80MS/s</td>
</tr>
<tr>
<td>Active Area</td>
<td>1.18mm x 0.54mm</td>
</tr>
<tr>
<td>Input Range</td>
<td>1.2Vp-p Differential</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>0.8V 1.2V</td>
</tr>
<tr>
<td>SNDR</td>
<td>55.0dB @2MHz 51.4dB @41MHz</td>
</tr>
<tr>
<td>Total Power Consumption</td>
<td>6.5mW 13.3mW</td>
</tr>
<tr>
<td>INL</td>
<td>&lt; 1.0LSB &lt; 0.5LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>&lt; 0.8LSB &lt; 0.4LSB</td>
</tr>
</tbody>
</table>

Fclk=80MS/s, Fin=11MHz

![Graph showing SNDR vs Supply Voltage for different temperatures and operating modes.](image)
Optimization of $V_{\text{eff}}$

Optimum $V_{\text{eff}}$ is a function of resolution, current, and design rule.

The lower $V_{\text{eff}}$ is recommended for scaled CMOS technology.

12 bit, 0.18um CMOS

10 bit

Red: 90nm

Blue: 0.18um
Challenge to realize pipelined ADC without OpAmp

Comparator controlled current source can realize the virtual ground.

Now challenge for not use of OpAmp in ADC design has started.

Conventional OpAmp

Comparator controlled current source

Realistic comparator controlled current source

Time delay \((V_x \rightarrow V_o)\) causes voltage offset. Small inverse current source has been introduced. The offset voltage can be reduced and does not affect the conversion linearity.

\[I_2 \ll I_1\]


10b, 8MHz ADC has been developed. 
Pd=2.5mW. Lowest Pd/MHz
Results

Small FoM, however not amazingly

10b ADC FoM = 0.3pJ/step, 0.3mW/MHz
Sub-ranging ADC

Sub-ranging ADC also doesn't require OpAmp and suitable for LV operation. However it requires low offset voltage comparators.

Use of positive feedback technique has realized low offset voltage.

Technology revival has been found.

Pd/MHz = 0.75mW/MHz which is lowest value!!

Results

Attain high ENOB of 10.5-11.0
30mW at 40MHz

90nm CMOS 1V Operation

0.4pJ/step
Successive approximation ADC

Successive approximation ADC has been used long time as a low power and low speed ADC. It doesn’t require OpAmp but capacitor array and comparator. Thus this architecture looks suitable for scaled and low voltage CMOS.

Now challenge for renewal of this conventional architecture has started.

Successive approximation ADC

SA-ADC

Eight interleaved SA-ADCs with 90nm CMOS attain 600MHz operation.

Improvement of SA-ADC

Asynchronous clock increases conversion frequency. Use of proper radix reduces capacitance.

Asynchronous clock

Tracking Phase  Synchronous Conversion Phase  Sampling Instants

MSB  MSB-1  MSB-2  ...  LSB

MSB  MSB-1  MSB-2  ...  LSB

Tracking Phase  Asynchronous Conversion Phase  Sampling Instants

Capacitor ladder with some radix number

$$\beta = 1 + \alpha \beta$$

$$\text{radix} = 1 + \frac{\beta}{\alpha}$$

6bit 600MHz 5.3mW ADC has been realized with 0.13um CMOS

Newest SAR ADC

SAR ADC must be one of the good solution for scaled analog technology.
No OPamp is needed.

No static power consumption.
Higher signal swing and small capacitance

\[ Q_{\text{REF}} = \sum_{i} 2^i C_U \cdot V_{DD} \]

Analog operation with capacitances

Capacitances can realize analog operation for SAR ADC. No static current is required and higher signal swing can be used.

\[ Q = \frac{C_S}{2} \times V_{IN} - 128 \cdot C_U \times V_{DD} + 64 \cdot C_U \times V_{DD} \pm \ldots \]
Results

Amazing small FoM=65fJ/step has been attained.

8bit, 0.3mW at 20MHz

J. Craninckx and G. Van der Plas,
“A 65fJ/Conversion-Step 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS,” IEEE ISSCC 2007, Dig. of Tech. Papers, pp.246-247, Feb. 2007.

<table>
<thead>
<tr>
<th>ISSCC06 Paper #</th>
<th>Arch.</th>
<th>Fs [MS/s]</th>
<th>ENOB</th>
<th>P [mW]</th>
<th>FoM [fJ]</th>
<th>FoM includes</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>CTΔΣ</td>
<td>40</td>
<td>12</td>
<td>50</td>
<td>300</td>
<td>-</td>
</tr>
<tr>
<td>3.4</td>
<td>ΔΣ</td>
<td>4.4</td>
<td>12.6</td>
<td>13.8</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td>12.1</td>
<td>PL</td>
<td>100</td>
<td>9.4</td>
<td>39</td>
<td>570</td>
<td>-</td>
</tr>
<tr>
<td>12.3</td>
<td>Subr.</td>
<td>50</td>
<td>10.4</td>
<td>30</td>
<td>440</td>
<td>-</td>
</tr>
<tr>
<td>12.4</td>
<td>PL–CBSC</td>
<td>7.9</td>
<td>8.7</td>
<td>2.5</td>
<td>760</td>
<td>-</td>
</tr>
<tr>
<td>12.5</td>
<td>SAR</td>
<td>0.1</td>
<td>10.5</td>
<td>0.025</td>
<td>170</td>
<td>No</td>
</tr>
<tr>
<td>12.7</td>
<td>PL</td>
<td>50</td>
<td>9.2</td>
<td>15</td>
<td>510</td>
<td>-</td>
</tr>
<tr>
<td>31.1</td>
<td>Flash</td>
<td>1250</td>
<td>3.7</td>
<td>2.5</td>
<td>160</td>
<td>-</td>
</tr>
<tr>
<td>31.5</td>
<td>SAR</td>
<td>300</td>
<td>5.3</td>
<td>2.65</td>
<td>220</td>
<td>No</td>
</tr>
<tr>
<td>This work</td>
<td>CS–SAR</td>
<td>20</td>
<td>7.8</td>
<td>0.29</td>
<td>65</td>
<td>Yes</td>
</tr>
</tbody>
</table>

The table above compares the FoM (figure of merit) metrics of different architectures for an ADC. The FoM is calculated as follows:

\[ \text{FoM} = \frac{\text{P}}{\text{ENOB} \times \text{Fs}} \]

where P is the power consumption, ENOB is the effective number of bits, and Fs is the sampling frequency. The table includes architectures such as CTΔΣ, ΔΣ, PL, Subr., PL–CBSC, SAR, Flash, and CS–SAR. The FoM is reported in fJ per conversion step for each architecture at different input frequencies.
High resolution and high speed SAR ADC

To increase the resolution, a pre-amplifier is located in front of a comparator.

Results

High conversion rate of 40MS/s and low power of 66mW have been attained.

High ENOB of 13.5 bit has been attained.

FoM = 0.14pJ/step

0.13um CMOS

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.5V</td>
</tr>
<tr>
<td>Input range</td>
<td>±0.9V diff.</td>
</tr>
<tr>
<td>Sample frequency</td>
<td>40MHz</td>
</tr>
<tr>
<td>Internal clock</td>
<td>480MHz</td>
</tr>
<tr>
<td>Analog power</td>
<td>49mW</td>
</tr>
<tr>
<td>Digital power</td>
<td>17mW</td>
</tr>
<tr>
<td>Total power</td>
<td>66mW</td>
</tr>
</tbody>
</table>
In delta-sigma ADC, higher operating frequency can increase SNR. For higher resolution ADC, the delta-sigma method must be vital.

Nyquist ADC:

\[ SNR \propto CV_{\text{sig}}^2 \]

Delta-sigma ADC:

\[ SNR \propto CV_{\text{sig}}^2 \cdot M^\alpha \]
Delta sigma ADCs have emerged as a strong rival to high resolution Nyquist ADCs.

90nm CMOS, BW=20MHz, DR (=SNR) = 77dB, 50mmW, FoM=200fJ/conv.


<table>
<thead>
<tr>
<th>Technology</th>
<th>90nm CMOS, 1P6M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Architecture</td>
<td>CT quadrature cascaded ΣΔ modulator (2-2, 4b)</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>340MHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>20MHz @ 10.5MHz IF</td>
</tr>
<tr>
<td>Max. input voltage</td>
<td>1Vp (differential)</td>
</tr>
<tr>
<td>Dynamic range*</td>
<td>77dB (97dB @ 200kHz, 115dB @ 3kHz)</td>
</tr>
<tr>
<td>Peak SNR / SNDR*</td>
<td>71dB / 69dB</td>
</tr>
<tr>
<td>Image rejection</td>
<td>&gt;55dB (for -1MHz input tone)</td>
</tr>
<tr>
<td>Active chip area</td>
<td>0.5mm²</td>
</tr>
<tr>
<td>Power consumption</td>
<td>50mW (analog), 6mW (digital)</td>
</tr>
<tr>
<td>Figure-of-merit (FOM)</td>
<td>0.2pJ/conv. (FOM=P/(2^enob<em>2</em>BW))</td>
</tr>
</tbody>
</table>

(*1MHz input signal, signal bandwidth is 20MHz)
Summary

- Technology issues due to technology scaling
  - Low voltage operation → small headroom
  - Reducing voltage gain
  - Small voltage swing → larger signal capacitance
  - Difficult to realize high resolution ADCs

- Design challenges of ADCs
  - Pipelined ADC
    - Optimization of OpAmp
    - Comparator controlled current source
  - Revival of ADC architectures
    --- No use of OpAmps ---
    - Sub-ranging ADC
    - SAR ADC
  - Delta-sigma ADC is increasing signal bandwidth