Compensation techniques for integrated analog device issues

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2007.09.20 SSDM A. Matsuzawa
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Integrated analog devices

Analog circuits need many passive devices, as well as transistors

MOS Transistor
Resistor
Capacitor
Inductor
Characteristics of passive devices

Passive components has some imperfections

<table>
<thead>
<tr>
<th></th>
<th>Diffusion Resistance</th>
<th>Poly Resistance</th>
<th>Poly to Poly Capacitance</th>
<th>Gate Capacitance</th>
<th>MIM Capacitance</th>
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<tr>
<td>Sheet R or C</td>
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<td>20-100 ohm</td>
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<td>2-5 fF/um²</td>
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<td>Absolute accuracy</td>
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<td>5-10</td>
<td>2-5</td>
<td>5-10</td>
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<td>(3sigma; %)</td>
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<tr>
<td>(3sigma; %)</td>
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<tr>
<td>(%/V)</td>
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<td>Comment</td>
<td>Large VC Leak</td>
<td>Low VC</td>
<td>Low VC Cost up</td>
<td>High VC</td>
<td>Good Q (RF)</td>
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<td>Low leak</td>
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<td>Cost up</td>
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$V_T$ mismatch

$V_T$ mismatch causes offset voltage of an amplifier and a comparator. Larger gate area is needed to reduce offset voltage, however results in decrease of performances, such as BW and PD.

\[ \Delta V_T (mV) \]

\[ LW(\mu m^2) \]

0.13um: Morifuji, et al., IEDM 2000
0.4um : My data

\[
(\Delta V_T)^2 \propto \frac{T_{OX}^2}{LW}
\]

\[
\Delta V_T \propto \frac{T_{ox}}{\sqrt{LW}}
\]
$V_T$ fluctuations in a wafer

$V_T$ fluctuation for small device looks random in a wafer. $V_T$ fluctuation for large device have some gradients in a wafer.

$V_t = 575 \pm 18 \text{mV}$

$V_t = 686 \pm 7 \text{mV}$
Influence of $V_T$ mismatch in current staring DAC

Higher resolution DAC requires smaller current mismatch which is mainly caused by $V_T$ mismatch.

\[ \sigma(I) \approx \frac{1}{2C\sqrt{2^N}} \]

$N$: resolution
$C$: Constant determined by INL

\[
\left( \frac{\sigma(I)}{I} \right)^2 \propto \frac{1}{2^N}
\]
Issue in high precision analog design

High precision analog circuit design conventionally results in increase of power dissipation and IP cost, decrease of frequency performance.

- Large power dissipation
- Large capacitance
- Expensive cost
- Large area
- Low cutoff frequency
- Large capacitance

High precision circuits → Small mismatch → Large Gate size → Expensive cost → Large area → Low cutoff frequency → Large capacitance
Dynamic current compensation

Each current source can be set equal by current memory method. Shit register and one extra current source can realize calibration on the job.


16bit DAC

Shift register

Switch circuit

To D/A converter

Current source under calibration

Current memory

V_{DD}

I_{ref}

CAL

JOB

CAL: ON

JOB: OFF
Self-Calibrated DAC

CAL-ADC measures non-linearity of DAC and compensates its non-linearity by CAL-DAC with logic

Y. Cong and R. L. Geiger, Iowa State University, ISSCC 2003
Effectiveness and issues of CAL-DAC

Digital calibration can reduce non-linearity dramatically. We can realize high precision DAC in small area and power dissipation.

However, unrealistic, because it needs high precision ADC!!

14b 100MS/s DAC
1.5V, 17mW, 0.1mm², 0.13um
SFDR=82dB at 0.9MHz, 62dB at 42.5MHz

Area: 1/50 Pd: 1/20
We have developed self-calibrated Binary DAC without CAL-ADC. Comparator can calibrate non-linearity. No high precision ADC is needed.

Error compensation by comparator

Nature of binary weighted values

\[
\frac{1}{2^m} = \sum_{n=1}^{i} \frac{1}{2^{m+n}} + \frac{1}{2^{m+i}}
\]

\[
\frac{1}{2^4} = \frac{1}{2^5} + \frac{1}{2^6} + \frac{1}{2^7} + \frac{1}{2^8}
\]

1) Measure LSB value by CAL DAC with certain accuracy. \[\frac{I_o}{2^N}\]

2) Measure the error of each current source by comparator with binary search.

3) Compensate the errors by digitally

\[\delta I_m = \frac{I_o'}{2^m} - \sum_{n=1}^{N-m} \frac{I_o}{2^{m+n}} - \frac{I_o}{2^N}\]

\[\delta I_{13} = \frac{I_o'}{2^{13}} - \frac{I_o}{2^{14}} - \frac{I_o}{2^{14}}\]

\[\delta I_{12} = \frac{I_o'}{2^{12}} - \frac{I_o}{2^{13}} - \frac{I_o}{2^{14}} - \frac{I_o}{2^{14}}\]
Comparator and offset suppression

Store the offset voltage in capacitor and subtract it from the signal.

Offset suppression

- **V_{off}** at sigma reaches 30mV in CMOS comparator

(a) Low gain type (feed forward method)

(b) High gain type (feedback method)

Basic CMOS comparator

\[ (V_a - V_{os})(-A) = V_o = V_a \]

\[ V_o = V_a = \frac{A}{1 + A} V_{os} \]
Digital Comparator offset compensation

Offset voltage of latched comparator can’t be compensated by previous method. Because it has no bias point. In this case, digital method should be applied.

Input terminals are shorted and the output signal controls applied voltage to the differential pair in CAL circuits so that the frequency of occurrence in differential output signals become equal.

“"A 90nm CMOS 1.2V 6b 1GS/s Two-Step Subranging ADC”
Pedro M. Figueiredo et al., ISSCC 2006

C_{CAL} = 10 \ C_s
Capacitor mismatch in pipelined ADC determines the conversion accuracy. For the higher resolution, the larger capacitance is needed.

\[ V_o \approx 2V_{in} - V_{DAC} \]

\[ V_o \approx V_{in} \left( 1 + \frac{C_s}{C_f} \right) - \frac{C_s}{C_f} V_{DAC} \]

\[ \Delta V_o = \left( \frac{\Delta C_s}{C_s} - \frac{\Delta C_f}{C_f} \right) (V_{in} - V_{DAC}) \]

\[ \frac{\Delta C}{C} (\sigma) = \frac{2 \times 10^{-4}}{\sqrt{C_{(pF)}}} \]
Capacitor mismatch compensation

Capacitor mismatch causes the large conversion value differences at the input voltage where the comparator changes the DAC voltage.

Compensation method:

1) Select input signal to +/- \( V_{\text{ref}}/4 \)
2) Convert this value with \( V_{\text{DAC}}=0 \) and +/- \( V_{\text{ref}} \) and obtain \( \delta_1 \) and \( \delta_2 \).
3) Add or subtract this \( \delta_1, \delta_2 \) to or from the output values.

1/f noise degrades SNR of base-band signal seriously. The 1/f noise from MOS is one or two order of magnitude higher than bipolar. The larger gate area is needed to reduction this noise.

\[ S_{AVG} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \]
Chopper amplifier

Chopper technique is often to be used to reduce the effect of 1/f noise.


\[ S_{\text{Nout}}(f) = \left( \frac{2}{\pi} \right)^2 \sum_{n=-\infty}^{\infty} \frac{1}{n^2} |G(f - nf_s)|^2 S_{\text{Nin}}(f - nf_s) \]
Image-rejection mixers

Image can be rejected theoretically. However, the image still remains due to gain and phase mismatch.

\[ V_1(t) = -\frac{V_{\text{des}}}{2} \sin(\omega_{\text{des}} - \omega_{\text{LO}})t + \frac{V_{\text{im}}}{2} \sin(\omega_{\text{LO}} - \omega_{\text{im}})t \]

\[ V_2(t) = \frac{V_{\text{des}}}{2} \cos(\omega_{\text{des}} - \omega_{\text{LO}})t + \frac{V_{\text{im}}}{2} \cos(\omega_{\text{LO}} - \omega_{\text{im}})t \]

\[ V_1(t) \rightarrow 90^\circ \text{ shift} = V_3(t) = \frac{V_{\text{des}}}{2} \cos(\omega_{\text{des}} - \omega_{\text{LO}})t - \frac{V_{\text{im}}}{2} \cos(\omega_{\text{LO}} - \omega_{\text{im}})t \]

\[ V_{\text{out}}(t) = V_{\text{des}} \cos(\omega_{\text{des}} - \omega_{\text{LO}})t \]

Image is rejected, however,…
Gain mismatch and phase error

It is very difficult to realize high image rejection ratio being higher than 40 dB by analog techniques.

\[ \Delta \theta + \Delta G \approx \frac{(\Delta G)^2}{G} + (\Delta \theta)^2 \]

Conventional IRR: 35dB
IRR: Image rejection ratio

0.1 deg and 0.01% are needed for IRR of 60dB

The dummy image signal is generated by IMO and the controller controls signal delay and amplitude on Q path to minimize the I/Q imbalance. IRR of 60dB can be realized.
CT filter tuning

RC or gmC circuits can realize active filter circuits, However, frequency characteristics and Q of the filter are strongly affected by Absolute value of R, C, gm and PVT fluctuation. Then, the filter tuning circuit is vital. Filter circuit can be used as oscillator, if the Q become infinity.
Digital calibration in mixed signal SoC

To keep high production yield and stable operation against PVT fluctuation, mixed signal SoC has many digital self calibration circuits. MCU controls many analog parameters.

PRML circuit for DVD recorder
Issues of analog compensation techniques

• Basically use discrete-time technology
  – Difficult to apply Continuous-Time circuits.
  – Needed clock causes another noise.

• Some need calibration period
  – At power on
    • Needs not short time to wait the system becomes stable.
    • Some different situation at the power on.
  – Idling time on the job
    • Can get sufficient time for calibration?
    • Too much system depended.

• Calibration on the job
  – Conventionally needs extra circuits.
    Cost and power consumption increase.
  – Needs many calibration time, if statistical methods are used.
Conclusion

• Analog circuits require compensation technique
  – Mismatch is inversely proportional to the square root of area.

\[ \Delta V_T, V_{n-1/f}, \left( \frac{\Delta C}{C} \right), \left( \frac{\Delta R}{R} \right) \propto \frac{1}{\sqrt{S}} \]

  – Control of absolute value of device parameters is difficult.
  – Also, device parameters are affected PVT fluctuation easily.
  – If not use of compensation techniques
    • Large area, large power consumption, poor frequency performance.

• Compensation techniques are very effective to improve precision of circuits, production yield, and durability to PVT fluctuations

• However, they have many issues
  – Basically DT method are used and difficult to apply CT circuits.
  – Need calibration periods