A 14-bit 100-MS/s Digitally Calibrated Binary-Weighted Current-Steering CMOS DAC without Calibration ADC

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Outline

• Motivation
• The Calibration Scheme
• Measurement Results
• Conclusions
• To realize a high speed and high resolution DAC, it is necessary to utilize the calibration technique.
• Keep the total area small.
Outline

• Motivation

• The Calibration Scheme

• Measurement Results

• Conclusions
The CS DAC function

1. The CS DAC linearity is limited by current source mismatch.
2. The mismatch is measured by CALADC.
3. CALDAC corrects the error currents.
1. Mismatch currents of MSBDAC are measured by CALADC.
2. The error currents are stored in CALMEM.
3. CALDAC corrects the error current.

This scheme has 3 problems.
The problem of CALADC

- CALADC needs a high resolution, such as 16 bits
  1. Complexity
  2. Long calibration time
  3. Large area
The problem of CALMEM

- A lot of calibration memory, $2^N$ words are required.
  1. Slow operation speed
  2. Large area
The problem of CALDAC

- If we keep MAINDAC small, the mismatch becomes large.
- CALDAC needs a high resolution, such as 10 bits.
The proposed calibration

1. Mismatch currents are measured by the current comparator.
2. The error currents are stored in CALMEM, a lower capacity.
3. LSBDAC, in the part of MAINDAC corrects the error current.
The proposed CALADC

- By using a current comparator and SAR logic, the error currents can be measured like in a SAR ADC

1. Simplicity
2. Short calibration time
3. Small area
The proposed CALMEM

- \( N \) current sources instead of \( 2^N \) current sources
- CALMEM allows a lower capacity, \( N \) words instead of \( 2^N \) words

1. Fast operation speed
2. Small area
The proposed CALDAC

- The error currents of MSBDAC are corrected by LSBDAC, in the part of MAINDAC
- LSBDAC has a high resolution, such as 8bits
  1. Extra CALDAC allows a low resolution
  2. Small area
The proposed DAC

Output

6-bit Current Mirror

SAR Logic Memory

Calibrated

6-bit MSBDAC

8-bit LSBDAC

3-bit CALDAC

6-bit SUBDAC

14-bit MAINDAC

$I_{MSB5} 2^{13}$

$I_{MSB0} 2^{8}$

$I_{CMSB0} 2^{8}$

$I_{LSB7} 2^{7}$

$I_{LSB0} 2^{0}$

$I_{CAL2} 2^{1}$

$I_{CAL0} 2^{3}$

$I_{CCAL0} 2^{3}$

$I_{SUB5} 2^{2}$

$I_{SUB0} 2^{3}$

$I_{CSUB0} 2^{3}$
MSB dummy calibration

- Comparing MSB dummy current ($I_{CMSB0}$) with the sum of the LSBDAC and CALDAC current ($I_{LSBs}$)
- SUBDAC is controlled to cancel out the error current, $\delta_0$
- $\delta_0$ is obtained as a 6-bit digital value.
MSB dummy calibration

Comparing $I_{CMSB0}$ with the total current, $I_{LSBs}$. Current mirror mismatch and comparator offset are canceled by changing the switch position.
MSB calibration

- Comparing the lowest MSBDAC current \( (I_{MSB0}) \) with the MSB dummy current \( (I_{CMSB0}) \) calibrated by SUBDAC.
- LSB, CALDAC are controlled to cancel out the error current, \( \delta_1 \).
- \( \delta_1 \) is obtained as an 11 bit digital value.
MSB calibration

- Comparing $I_{MSB0}$ with $I_{CMSB0}$ calibrated by SUBDAC
- Current mirror mismatch and comparator offset are canceled by changing the switch position.
The conversion operation
The comparison with others

14-bit digital calibration scheme

<table>
<thead>
<tr>
<th>Conference</th>
<th>CALADC</th>
<th>CALDAC</th>
<th>MemoryBit</th>
<th>CALBit</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>VLSI'06</td>
<td>On Chip $\Sigma$ΔADC</td>
<td>8bDAC $\times 16$</td>
<td>8×16</td>
<td>4</td>
<td>2.88mm$^2$</td>
</tr>
<tr>
<td>ISSCC'03</td>
<td>Off Chip $\Sigma$ΔADC</td>
<td>8bDAC $\times 63$</td>
<td>8×63</td>
<td>6</td>
<td>*0.1mm$^2$</td>
</tr>
<tr>
<td>ISSCC'01</td>
<td>On Chip $\Sigma$ΔADC</td>
<td>12bitDAC</td>
<td>12×15</td>
<td>4</td>
<td>11.8mm$^2$</td>
</tr>
<tr>
<td>JSSCC'01</td>
<td>Current Comp.</td>
<td>6bDAC $\times 4$</td>
<td>6×4</td>
<td>4</td>
<td>1mm$^2$</td>
</tr>
<tr>
<td><strong>This Work</strong></td>
<td><strong>Current Comp.</strong></td>
<td><strong>6bDAC $\times 4$</strong></td>
<td><strong>11×6</strong></td>
<td><strong>6</strong></td>
<td><strong>0.74mm$^2$</strong></td>
</tr>
</tbody>
</table>
Outline

• Motivation
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• Measurement Results
• Conclusions
Layout (0.18um CMOS)

Current Sources & Current mirrors

Latch & Switch

Logic & Memory

Comparator

Output circuits

800um

900um

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The Measurement Results

Before Calibration
SFDR 69dBc

After Calibration
SFDR 83dBc

@100MSps
6kHz Signal

SFDR 14dBUP
The Measurement Results

- For high frequencies, SFDR degrades.
  
  It can be improved by return-to-zero circuits
# The Performance Summary

<table>
<thead>
<tr>
<th>Tecnology</th>
<th>0.18 um CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14 bit</td>
</tr>
<tr>
<td>Update Rate</td>
<td>100 MSps</td>
</tr>
<tr>
<td>Full-Scale Current</td>
<td>11.5 mA</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8 V</td>
</tr>
<tr>
<td>SFDR (Before Calibration)</td>
<td>69.2 dBc @fsig=6kHz</td>
</tr>
<tr>
<td>SFDR (After Calibration)</td>
<td>83.4 dBc @fsig=6kHz</td>
</tr>
<tr>
<td></td>
<td>46.6 dBc @fsig=30MHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>79.2 mW (analog)</td>
</tr>
<tr>
<td></td>
<td>5 mW (digital)</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.74 mm²</td>
</tr>
</tbody>
</table>
Outline

• Motivation
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• Conclusions
The Comparison with other DACs

![Graph comparing Update Rate/Power (MSps/mW) vs. Active Area (mW)]

- ISSCC'04
- ISCAS'06
- VLSI'06
- VLSI'07
- This Work
- JSSCC'00
- JSSCC'99

Legend:
- ISSCC'04
- ISCAS'06
- VLSI'06
- VLSI'07
- This Work
- JSSCC'00
- JSSCC'99
Conclusions

• A new digital calibration scheme for a current-steering DAC has been proposed.

• By using a current comparator and the LSB part of the DAC for error correction, the additional circuits are kept minimal.

• Before calibration, the SFDR is 69.2 dBc. After calibration, the SFDR is greatly improved to 83.4 dBc.
Thank you for your interest

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The Simulation Results

Before Calibration

INL > 6 LSB

DNL > 6 LSB

After Calibration

INL < 0.5 LSB

DNL > 0.3 LSB
The Measurement Circuit

Agilent 16903A
Pattern Generator

Agilent 16903A
Clock

Start
14bData

Developed DAC

560Ω
270Ω
270Ω
THS4271

200Ω

560Ω

Tektronix TDS3044B

ADVANCEST R3267

Digital Oscilloscope

Spectrum Analyzer

or
MSB Calibration 2

\[ 2^9 I + \delta_1 \]

\[ 2^9 I + \delta_2 \]

\[ \delta_{1-2} \]

\[ 2^{8} I + \delta_1 \]

\[ 2^{8} I + \delta_2 \]

\[ -\delta_0 \]
**MSB Calibration**

\[ \delta_2 = \delta_1 - \frac{I_{CALA} - I_{CALB}}{2} \]

\[ \delta_{N+1} = \sum_{i=1}^{N} \delta_i - \frac{I_{CALA} - I_{CALB}}{2} \]