Nano-scale CMOS and Low Voltage Analog to Digital Converter Design Challenges

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4. Summary
Pipeline ADC is the major conversion architecture for communications and digital consumer products.
Pipeline ADC

Folding I/O characteristics makes higher resolution along with pipeline stages.
Speed and power

Conversion speed has saturated at 200 MHz
Smaller mW/MHz is needed for low power operation.
0.3mW/MHz for 10bit and 1mW/MHz for 12bit are the bottom lines.

![High Speed ADC](chart)

- **12Bit (Paper)**
- **10Bit (Paper)**
- **12Bit Products**
- **10Bit Products**

JSSC, ISSCC, VLSI, CICC, ESSCC & Products

1995-2006

- 12bit : 1mW / MHz
- 10bit : 0.3mW / MHz

200MHz
Effect of technology scaling on analog performance

Technology scaling and performance of pipeline ADC
Operating voltage trend

Operating voltage of scaled device will keep about 1V

- Analog High
- Analog Low
- Digital High
- Digital Low (Low leak)

About 1V operation

ITRS 2001

Low Standby Power
High Performance

ITRS 2003

Design Rule
Operational amplifier for ADC

Pipeline ADC needs high performance amplifier. The output signal range will be reduced along with voltage lowering.

\[ V_{in}^+ \]
\[ V_{in}^- \]
\[ V_{out}^+ \]
\[ V_{out}^- \]

Gain Boost amp.

\[ Vin \]
\[ V_{out} \]
\[ V_{dd} \]

\[ 2V_{eff} \]

Output signal range

\[ V_s = V_{dd} - 0.7V \]
\[ V_s = 0.5V \text{ @} V_{dd} = 1.2V \]
\[ V_s = 0.3V \text{ @} V_{dd} = 1.0V \]
Requirements for operational amplifier

Higher resolution requires higher open loop gain.
Higher conversion frequency requires higher closed loop GBW.

\[
G_{error} \approx -\frac{1}{G} \left( 2 + \frac{C_p}{C_f} \right) \approx -\frac{1}{G \beta}
\]

\[
\frac{1}{G} \leq \frac{\beta}{2^{N-M+1}}
\]
N: ADC resolution
M: Stage resolution

\[
G(dB) > 6N + 10 \quad \text{for 1.5b pipeline ADC}
\]

Closed loop gain-bandwidth

\[
\text{GBW}_{\text{close}} = \frac{g_m \beta}{2\pi C_L} > \frac{N \cdot f_c}{3}
\]

\[
\beta = \frac{C_f}{C_f + C_s + C_{pi}}
\]

\[
C_L = C_{po} + C_{ol} + \frac{C_f (C_s + C_{pi})}{C_f + C_s + C_{pi}}
\]

2006.10.25.
A. Matsuzawa, Tokyo Tech.
Larger SNR requires larger capacitance and larger signal swing. Low signal swing increases required capacitance.

\[ v_n^2 = \frac{n kT}{C} \quad \text{n: configuration coefficient} \]

\[ \text{SNR(dB)} = 10 \log \left( \frac{CV_{FS}^2}{8nkT} \right) \]

\[ \langle v_n^2 \rangle = 4kTR \int_0^\infty \frac{1}{1 + (\omega CR)^2} \frac{d\omega}{2\pi} = \frac{kT}{C} \]
Gain bandwidth of OpAmp increases along with technology scaling. However, can we increase every needed performances for ADCs?
Technology scaling can reduce parasitic capacitances. However signal capacitance will increase to keep the same SNR at lower voltage operation.

**Parasitic capacitance → smaller**
**Operating voltage → lower**
**Signal swing → lower**

**Signal capacitance → larger**
**Voltage gain → lower**

**Technology scaling**

\[ V_{\text{sig}} : \text{large} \]

\[ V_{\text{sig}} : \text{small} \]
Performance model for pipeline ADC

We have developed the performance model for pipeline ADC that can treat technology scaling.

\[ GBW_{\text{close}} = \frac{\frac{g_m}{2\pi}}{C_o} \left( 2 + \frac{C_{pi}}{C_o} + \frac{C_{po}}{C_o} + \frac{C_{pi}}{C_o} \right) \]
Scaling and analog device and circuit parameters

Gate width and capacitances decrease with technology scaling.

\[ V_{\text{eff}} = 0.175 \text{V} \]
\[ W = \frac{2L}{\mu C_{\text{ox}} V_{\text{eff}}^2 I_{\text{ds}}} \]

### Table (a)

<table>
<thead>
<tr>
<th>DR</th>
<th>( W_N )</th>
<th>( W_P )</th>
<th>( V_{A_N} )</th>
<th>( V_{A_P} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>24.3</td>
<td>74.9</td>
<td>0.82</td>
<td>0.69</td>
</tr>
<tr>
<td>0.13 ( \mu \text{m} )</td>
<td>37.5</td>
<td>147</td>
<td>0.82</td>
<td>0.64</td>
</tr>
<tr>
<td>0.18 ( \mu \text{m} )</td>
<td>54.8</td>
<td>219</td>
<td>0.99</td>
<td>0.93</td>
</tr>
<tr>
<td>0.25 ( \mu \text{m} )</td>
<td>116.0</td>
<td>396</td>
<td>0.78</td>
<td>0.97</td>
</tr>
<tr>
<td>0.35 ( \mu \text{m} )</td>
<td>162.0</td>
<td>603</td>
<td>1.01</td>
<td>0.86</td>
</tr>
</tbody>
</table>

### Table (b)

<table>
<thead>
<tr>
<th>DR</th>
<th>( C_{\text{plN}} )</th>
<th>( C_{\text{plP}} )</th>
<th>( C_{\text{po}} )</th>
<th>( \omega_{p2,N} )</th>
<th>( \omega_{p2,P} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>23.7</td>
<td>93.4</td>
<td>94.5</td>
<td>9.35</td>
<td>15.4</td>
</tr>
<tr>
<td>0.13 ( \mu \text{m} )</td>
<td>65.5</td>
<td>249</td>
<td>168</td>
<td>7.7</td>
<td>10.3</td>
</tr>
<tr>
<td>0.18 ( \mu \text{m} )</td>
<td>115</td>
<td>475</td>
<td>340</td>
<td>2.06</td>
<td>4.7</td>
</tr>
<tr>
<td>0.25 ( \mu \text{m} )</td>
<td>236</td>
<td>662</td>
<td>832</td>
<td>0.83</td>
<td>1.7</td>
</tr>
<tr>
<td>0.35 ( \mu \text{m} )</td>
<td>303</td>
<td>1034</td>
<td>892</td>
<td>0.54</td>
<td>1.7</td>
</tr>
</tbody>
</table>
Determination of signal capacitance

Larger resolution requires larger signal capacitance. Furthermore, Voltage lowering increases signal capacitance more.

\[ C_o \geq 1.66 \times 10^{-19} \left( \frac{2^N}{V_{sig}} \right)^2 \]

<table>
<thead>
<tr>
<th>90nm</th>
<th>0.13 μm</th>
<th>0.18 μm</th>
<th>0.25 μm</th>
<th>0.35 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{dd} )</td>
<td>1.2V</td>
<td>1.5V</td>
<td>1.8V</td>
<td>2.5V</td>
</tr>
<tr>
<td>( V_{sig,pp} )</td>
<td>1.0V</td>
<td>1.6V</td>
<td>2.2V</td>
<td>3.6V</td>
</tr>
</tbody>
</table>
Performance curve

Performance exhibits convex curve. There is the peak conversion frequency and the optimum current. Current increase results in increase of parasitic capacitances and decrease of conversion frequency in the higher current region.

\[ GBW_{\text{close}} = \frac{g_m}{2\pi C_o} \left( \frac{1}{2 + \frac{C_{pi}}{C_o}} + \frac{1}{1 + \frac{C_{po}}{C_o}} \right) + \frac{1}{1 + \frac{C_{pi}}{C_o}} \]

\[ g_m = \frac{2I_{ds}}{V_{eff}}, \quad C_{pi} = \alpha_i I_{ds}, \quad C_{po} = \alpha_o I_{ds} \]

\[ \begin{align*}
\text{①} & \quad C_o > C_{po}, C_{pi} \\
\text{②} & \quad C_{pi} < C_o < C_{po} \\
\text{③} & \quad C_o < C_{po}, C_o < C_{pi}
\end{align*} \]

\[ GBW_{\text{close}} \approx \frac{1}{\pi C_o V_{eff}} \cdot \frac{1}{3 + \alpha_o} \quad (\text{Constant}) \]

\[ GBW_{\text{close}} \approx \frac{1}{\pi C_o V_{eff}} \cdot \frac{1}{3 + \alpha_i \alpha_o I_{ds}} \quad (\propto \frac{1}{I_{ds}}) \]
0.13μm attains highest conversion frequency in a low current region. However, 90nm is overstriding 0.13μm along with increase of the current.
10 bit

The best design rule depends on operating current. 0.35μm attains highest conversion frequency in low operating current region!
12 bit

Relaxed design rule is suitable for wider current range.
14 bit

Scaled CMOS is not suitable for higher resolution ADC.
Performance summary

Scaled CMOS is effective for just low resolution ADC.
Scaled CMOS is not effective for high resolution ADC.
Voltage gain

$V_A$ decreases with scaling and operating voltage lowering. High gain can not be expected.

\[
G_i = g_m \cdot r_{ds} \quad g_m = \frac{2I_{ds}}{V_{eff}}, \quad r_{ds} = \frac{V_A}{I_{ds}} \quad G_i = \frac{2V_A}{V_{eff}} \approx 10V_A
\]
Voltage gain of operational amplifier

Voltage gain of OpAmp for scaled CMOS and LV operation is 80dB at most. 

Less than 10 bit ADC can be designed with scaled and low voltage CMOS.

\[ V_{ds} \approx V_{eff} \approx 0.2V \]

\[ G_i = \frac{2V_A}{V_{eff}} \approx \frac{2}{0.2} = 20dB \]
Design challenges for ADC in nano-scale era

--- No use of Operational amplifier  --

- Comparator controlled current source
- Successive approximation ADC
- Sub-ranging ADC
**Design rule and Speed in Comparator**

Gain bandwidth (=Speed) is inversely proportional to the $L^2$ (channel length). Technology scaling is still effective to increase the comparator speed and to reduce operating current. Furthermore, low voltage operation, such as 0.5V, is available.

$$GBW = \frac{g_m}{2\pi \left(WC_j + \frac{2}{3}C_{ox}LW\right)} = \frac{I_{sink}}{2\pi \left(WC_j + \frac{2}{3}C_{ox}LW\right)V_{eff}}$$

$$I_{sink} = \frac{\mu C_{ox} W V_{eff}^2}{2L}$$

$$C_{ox} = \frac{\kappa}{L}$$

![Comparator Circuit Diagram](attachment:image.png)

**Relative Bandwidth vs. Feature Size**

![Graph](attachment:graph.png)
Comparator controlled current source can realize the virtual ground.

Now challenge for not use of OpAmp in ADC design has started.

Realistic comparator controlled current source

Time delay \((V_x \rightarrow V_o)\) causes voltage offset. Small inverse current source has been introduced. The offset voltage can be reduced and does not effect the conversion linearity.

\[ I_2 << I_1 \]


10b, 8MHz ADC has been developed. Pd=2.5mW. Lowest Pd/MHz
Successive approximation ADC

Successive approximation ADC has been used long time as a low power and low speed ADC. It doesn’t require OpAmp but capacitor array and comparator. Thus this architecture looks suitable for scaled and low voltage CMOS.

Now challenge for renewal of this conventional architecture has started.

Eight interleaved SA-ADCs with 90nm CMOS attain 600MHz operation.

Improvement of SA-ADC

Asynchronous clock increases conversion frequency.
Use of proper radix reduces capacitance.

Asynchronous clock

Capacitor ladder with some radix number

6bit 600MHz  5.3mW ADC has been realized with 0.13um CMOS

\[ \beta = 1 + \alpha \beta \]

\[ \text{radix} = 1 + \frac{\beta}{\alpha} \]

Sub-ranging ADC

Sub-ranging ADC also doesn't require OpAmp and suitable for LV operation. However it requires low offset voltage comparators. Use of positive feedback technique has realized low offset voltage.

Technology revival has been found.

Pd/MHz = 0.75mW/MHz which is lowest value!!

Summary

• Technology scaling is effective for increasing analog performance if not so much higher SNR is required.

• Technology scaling is not effective for increasing analog performance if higher SNR is required, and sometimes degrades it.

• Increase of signal capacitance to keep the SNR high at low voltage operation is essential serious issue for use of scaled CMOS.

• Furthermore, Gain lowering of OpAmp due to technology scaling and voltage lowering becomes serious issues.

• Design challenges for ADC has been started.

• No use of OpAmp is a common idea.

• Technology revivals have been found and the performance has been improved. Further improvement will be expected in future.