Technology Trend of Ultra-High Data Rate Wireless CMOS Transceivers

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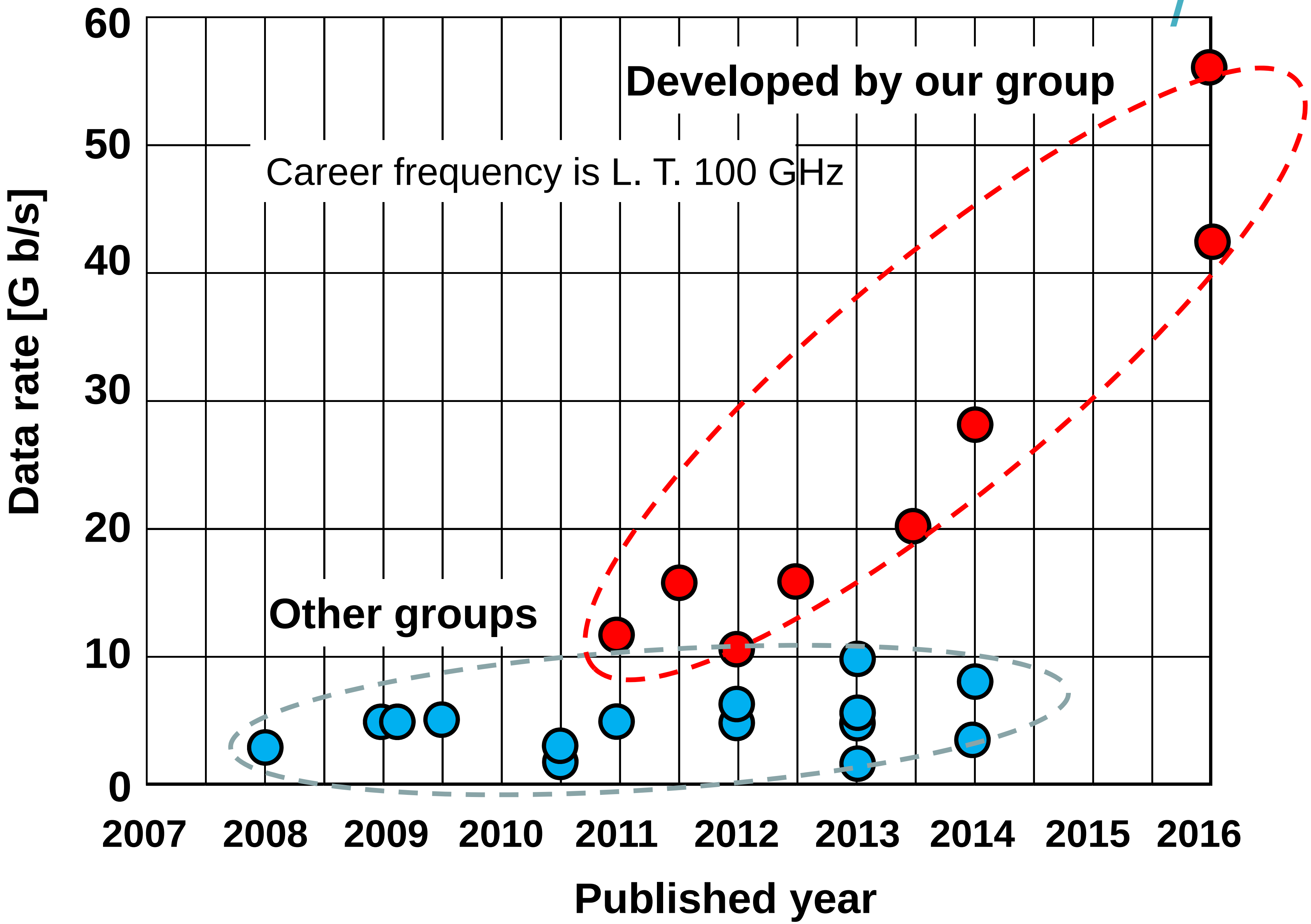
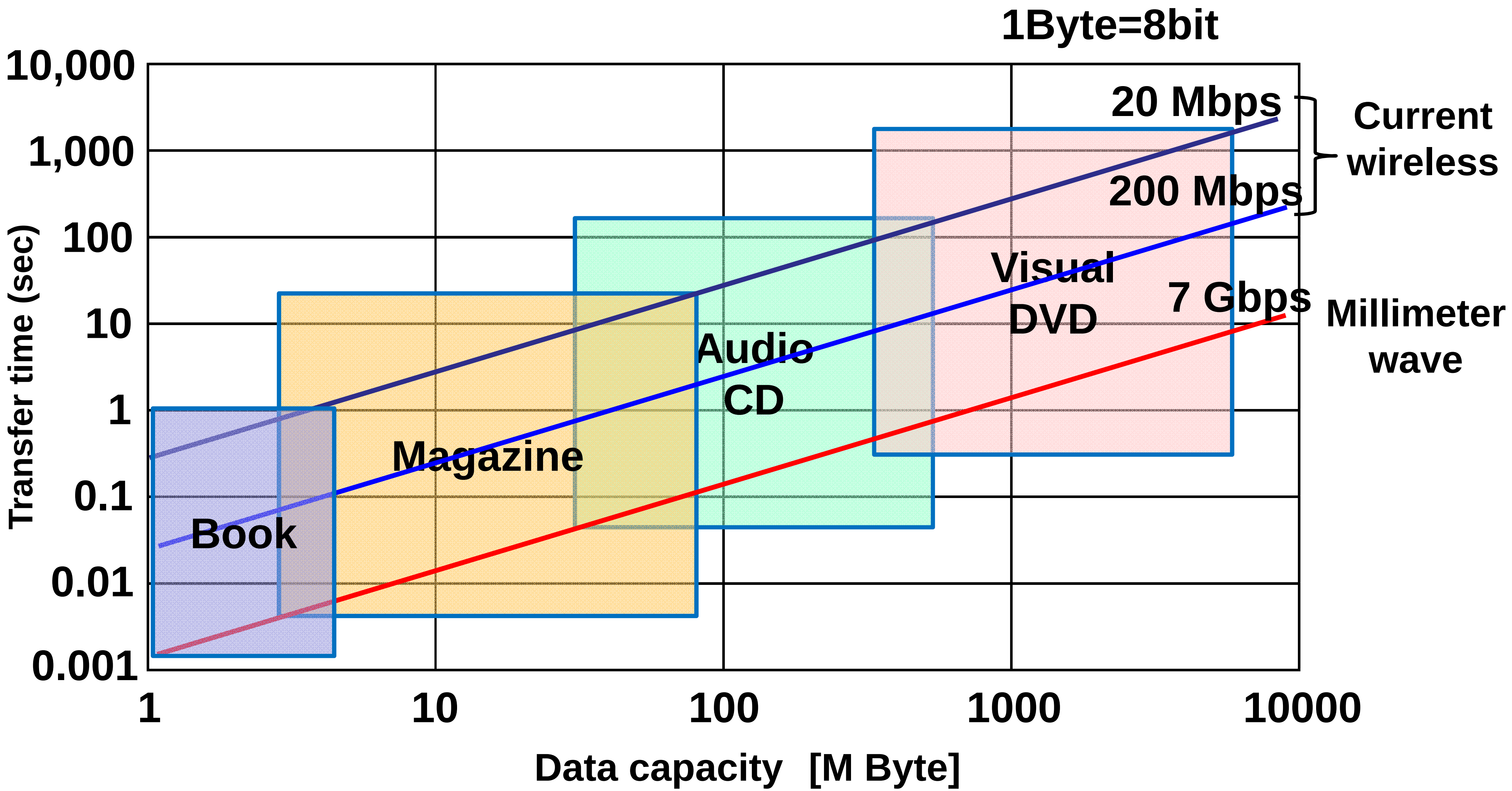
Demand for high speed data transfer

Progress of data rate in 60 GHz TRX



Transfer time vs. Data capacity

Transfer time of big contents can be reduced by increasing the data-rate. Millimeter wave can realize several second transfer of movie film in DVD.



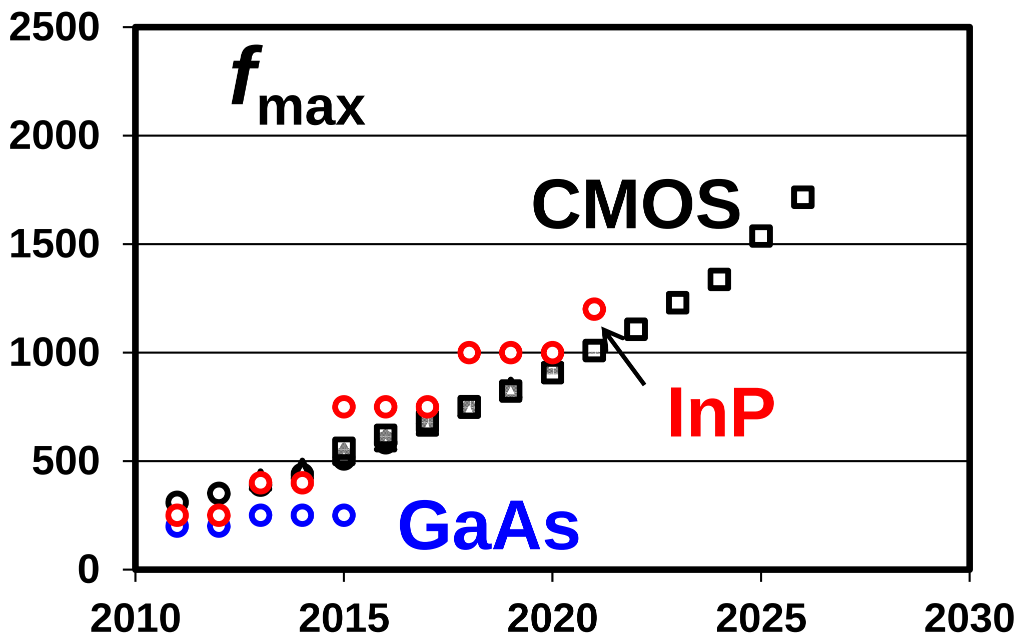
Our developed high data-rate mm Wave transceivers

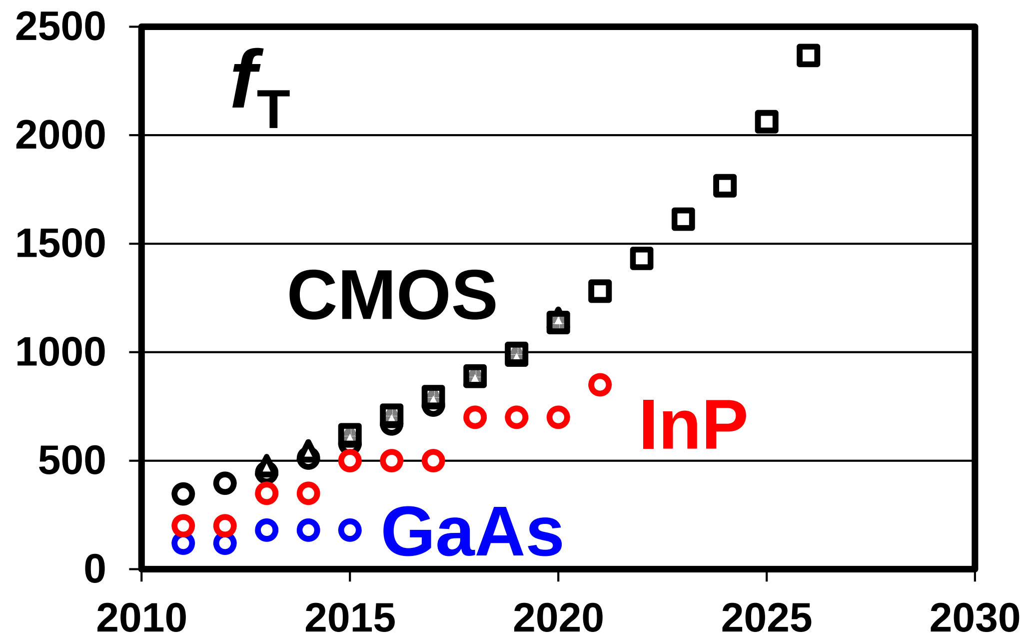
High freq. operation of semiconductor devices

f_T and f_{max} of CMOS are increased by technology scaling

$$G_{max} \approx \frac{f_{max}}{f_c}$$

$$NF_{min} \approx 1 + \left(\frac{f_c}{f_T}\right)\sqrt{1.3 g_m (R_g + R_s)}$$



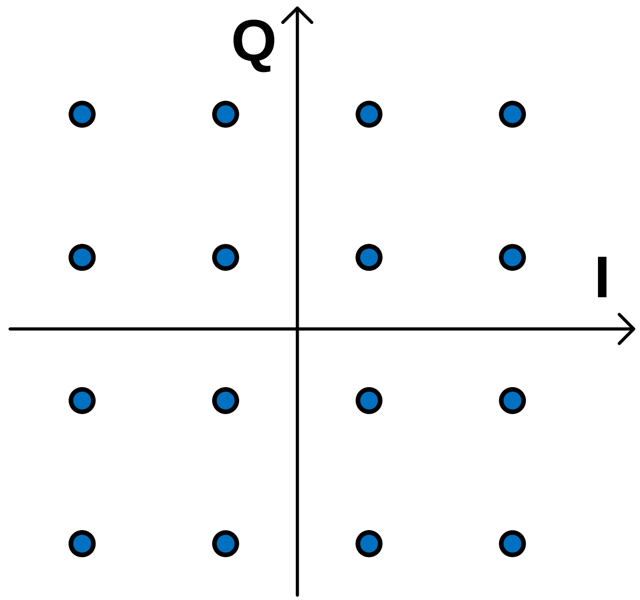


○ Bulk CMOS
△ Ultra-Thin-Body Fully-Depleted (UTB FD) SOI
□ Multi-Gate MOSFETs

Ultra-high speed data transfer in 60GHz band

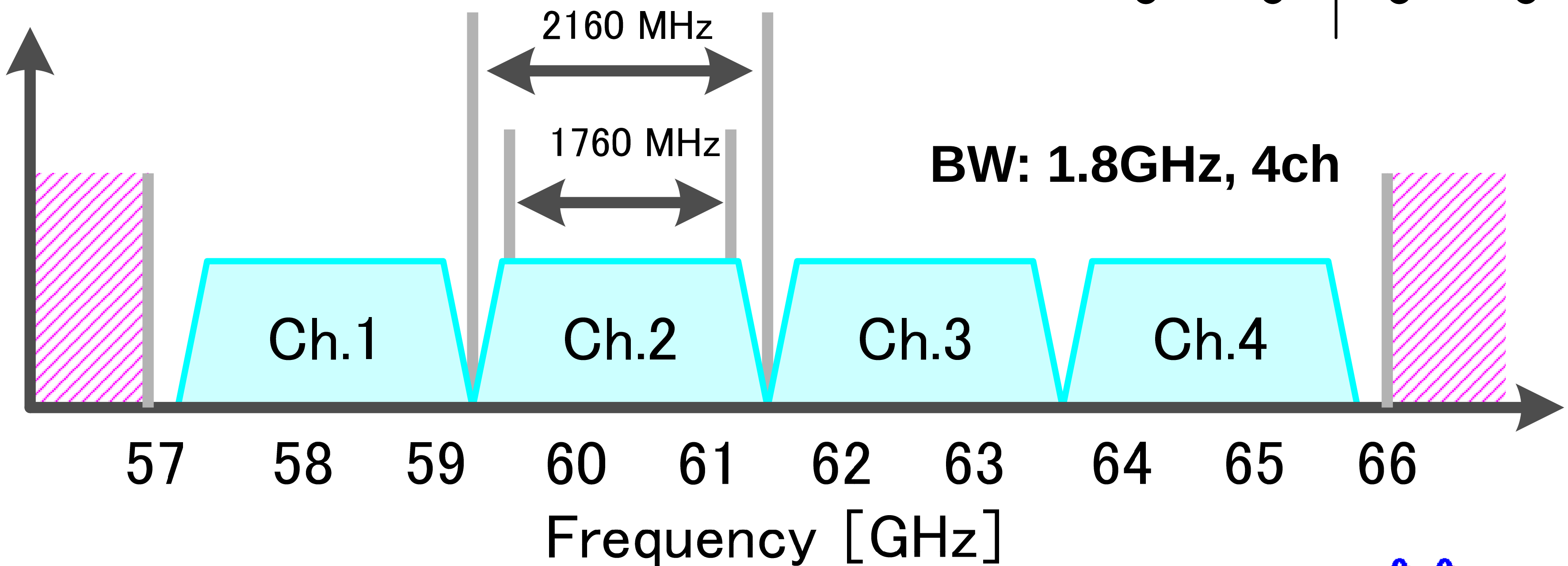
Wider BW and high # of bits are required

16QAM



BPSK: 1.7 Gbps
QPSK: 3.5 Gbps
16QAM: 7 Gbps
64QAM:10.5Gbps

$$D_{rate} \approx N \cdot BW$$



60GHz CMOS transceiver attained 28Gbps

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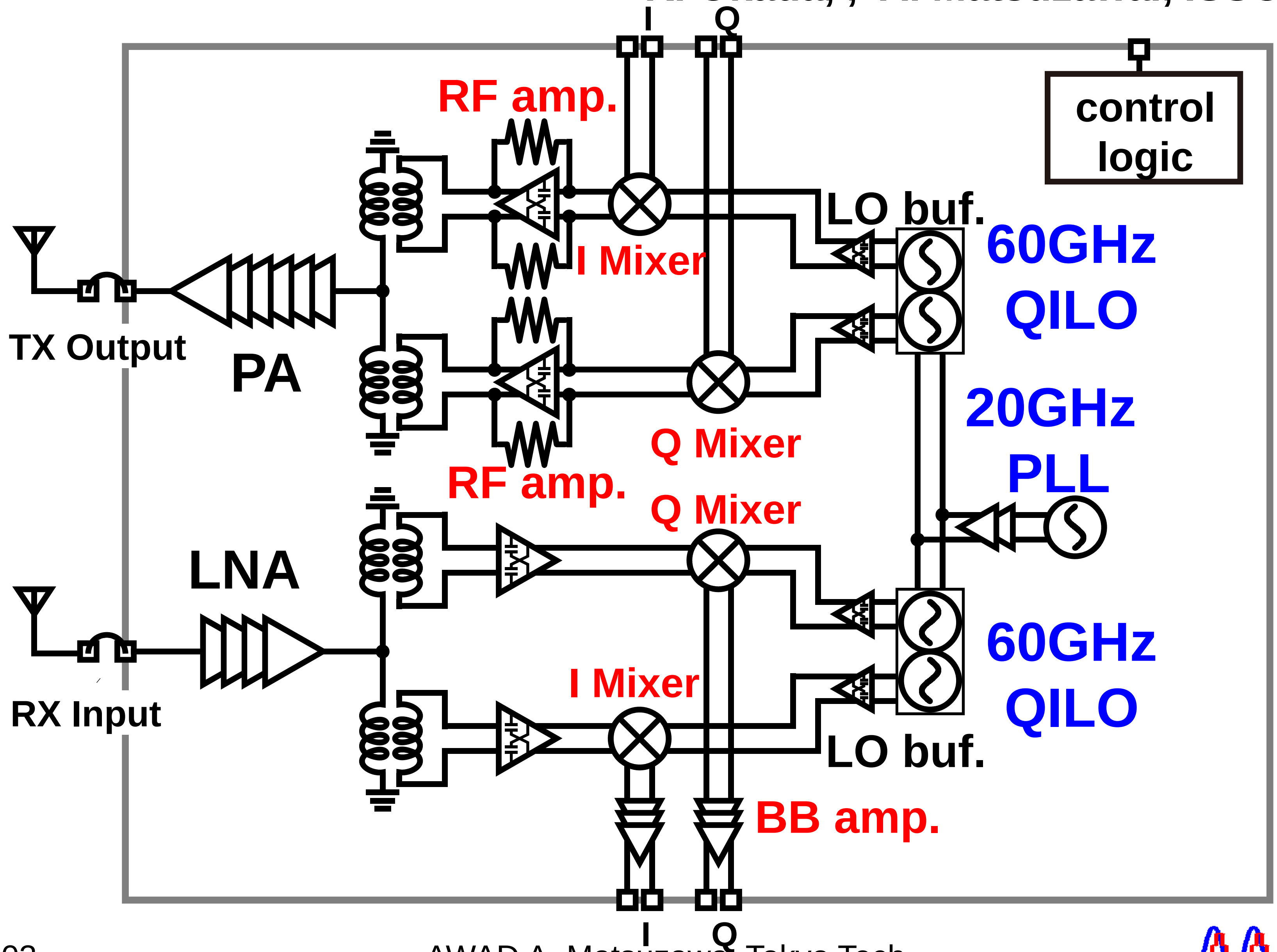
Direct conversion 60GHz CMOS transceiver

*K. Okada, , A. Matsuzawa., ISSCC 2014



Matsuzawa & Okada Lab.

Chip photo

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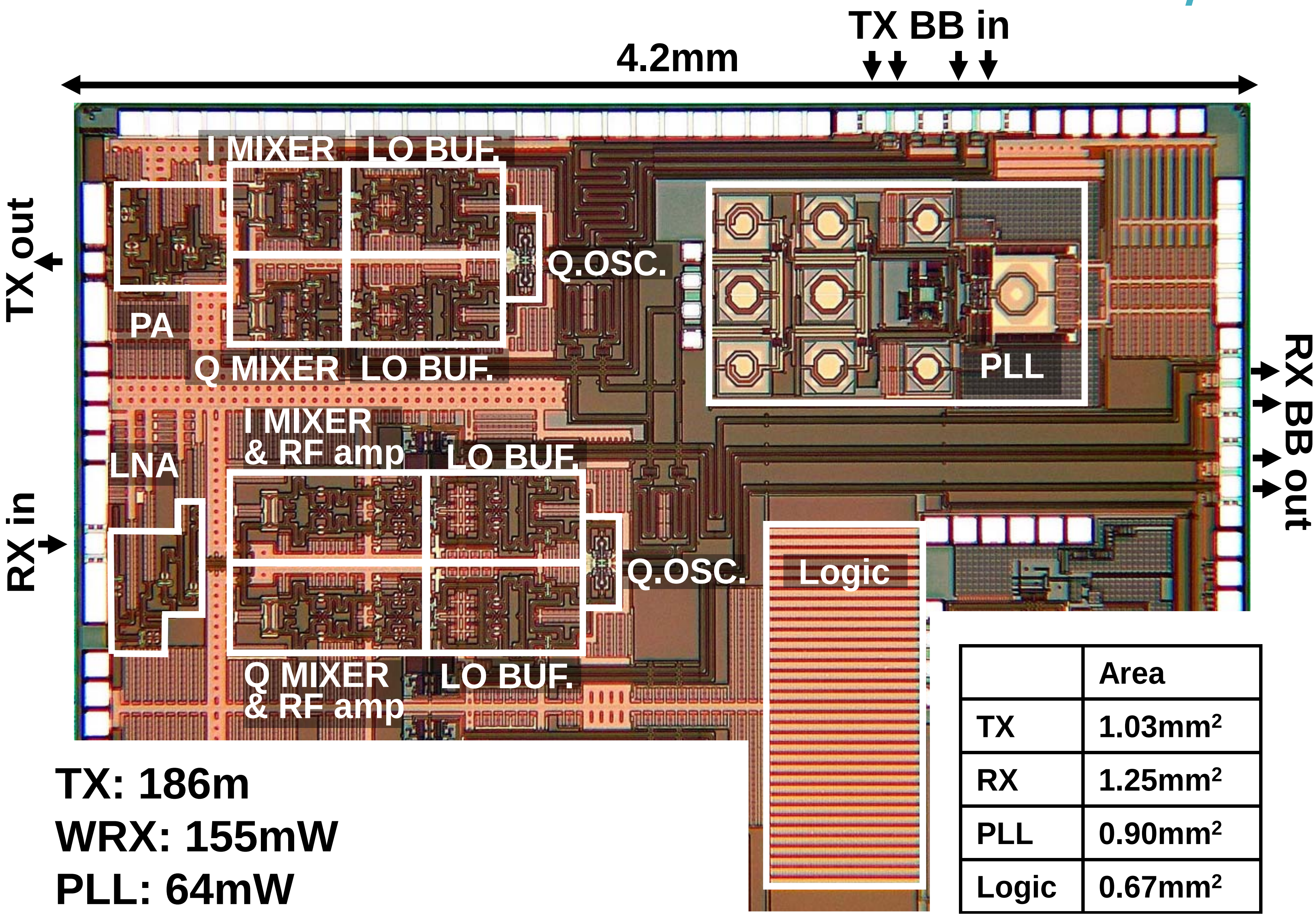
FUJITSU 65nm CMOS



	Area
TX	1.03mm^2
RX	1.25mm^2
PLL	0.90mm^2
Logic	0.67mm^2

TX: 186m
WRX: 155mW
PLL: 64mW

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Measured characteristics

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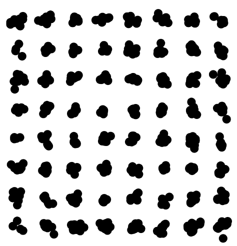
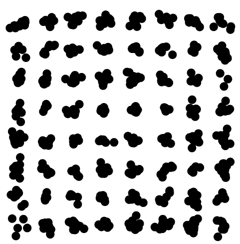
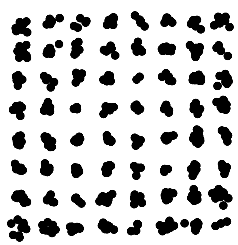
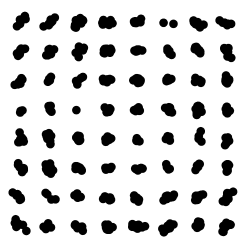
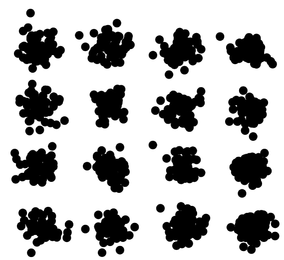
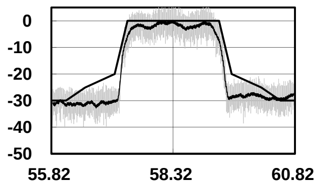
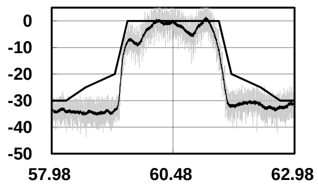
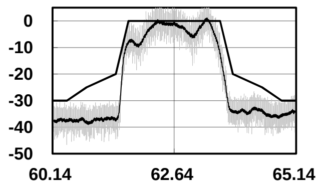
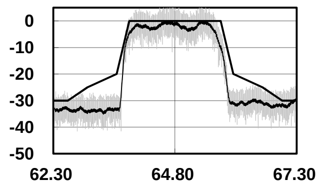
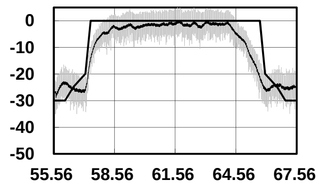
World's first 64QAM World’s fastest 28Gbps

Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 Channel bond
Modula-tion	64QAM				16QAM
Data rate*	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s	28.16Gb/s
Constella-tion**					
Spec-trum**					
TX EVM**	-27.1dB	-27.5dB	-28.0dB	-28.8dB	-20.0dB
TX-to-RX EVM***	-24.6dB	-23.9dB	-24.4dB	-26.3dB	-17.2dB

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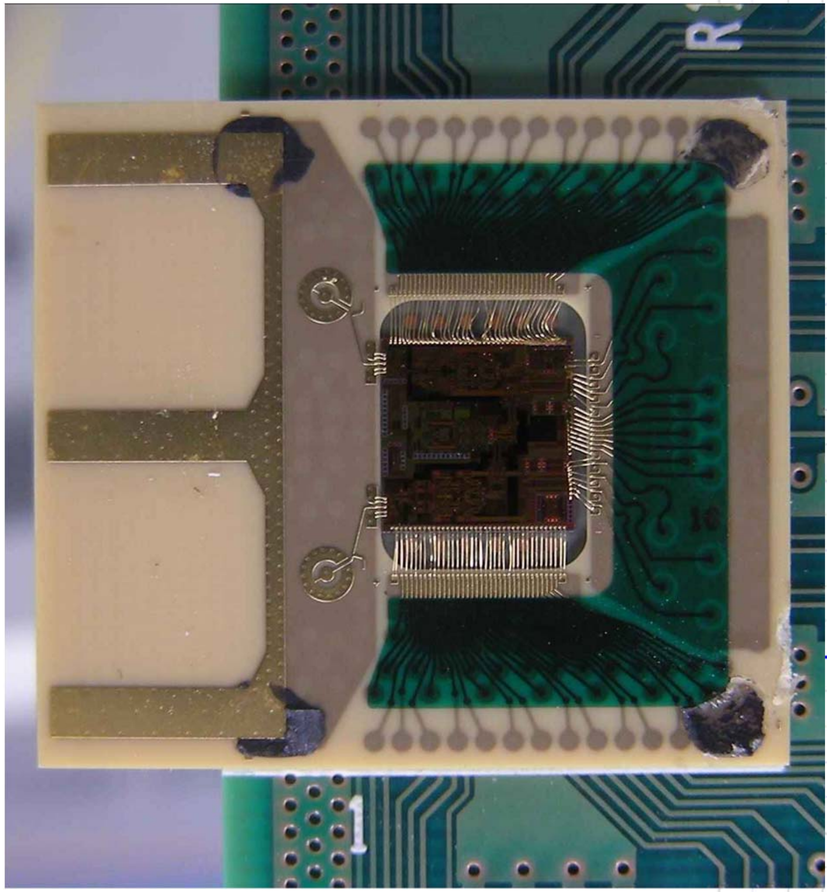
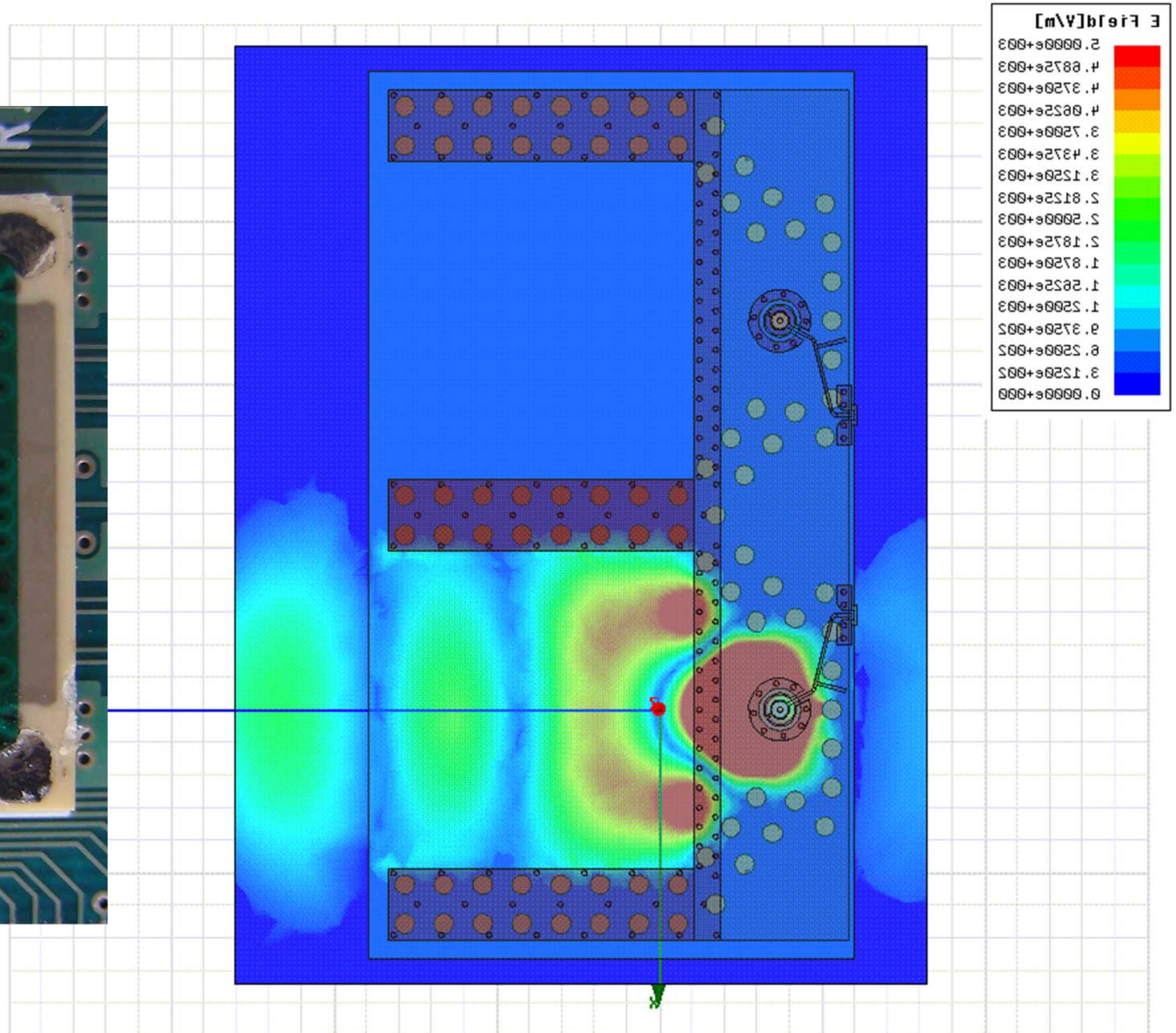
Chip with antenna in package

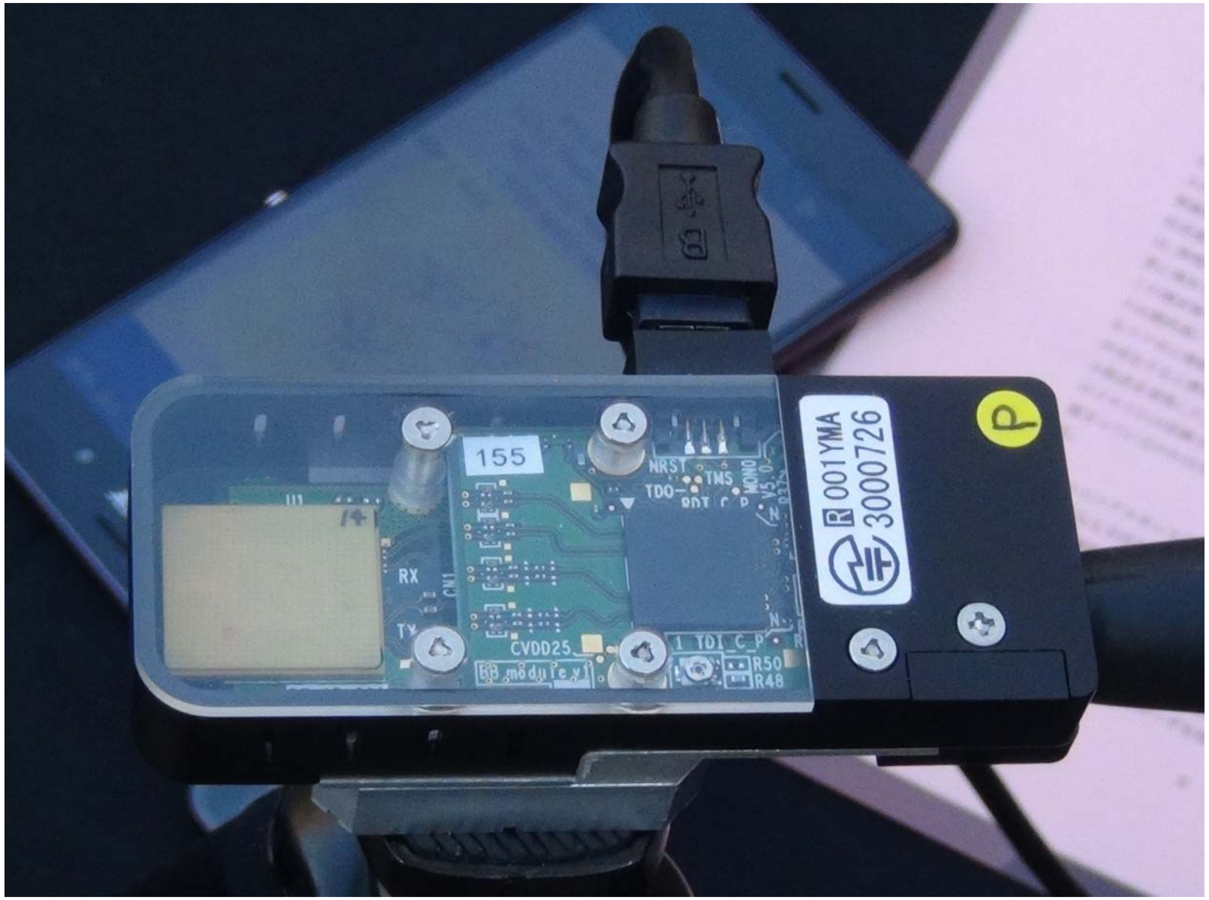
The 60GHz RF chip are mounted on the antenna in package



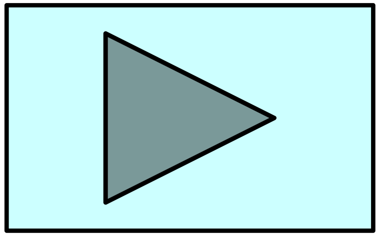


Recent developed 60GHz transceiver set

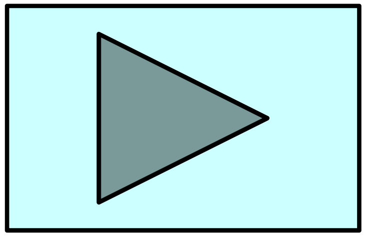
Small size 60GHz transceiver set has been developed.
It attains 6Gbps data transfer.



Smart phone

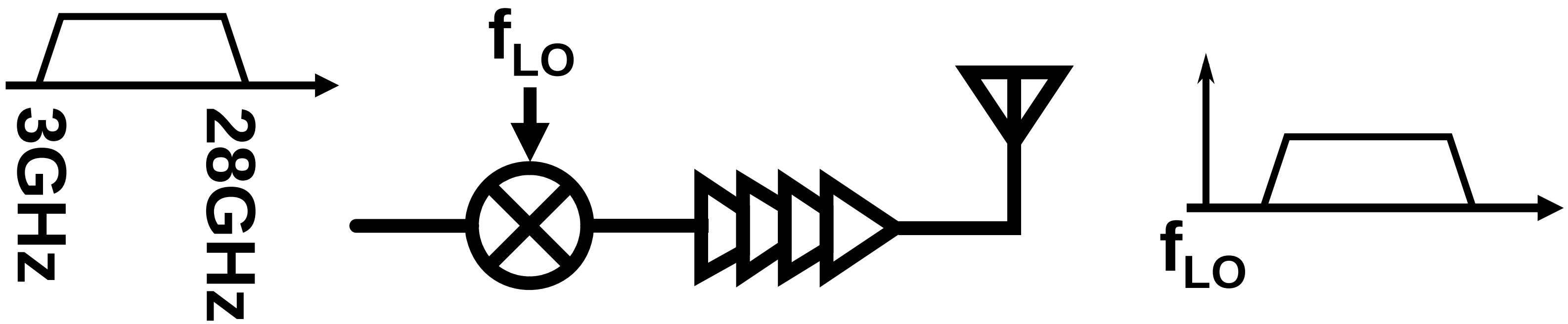


Gate



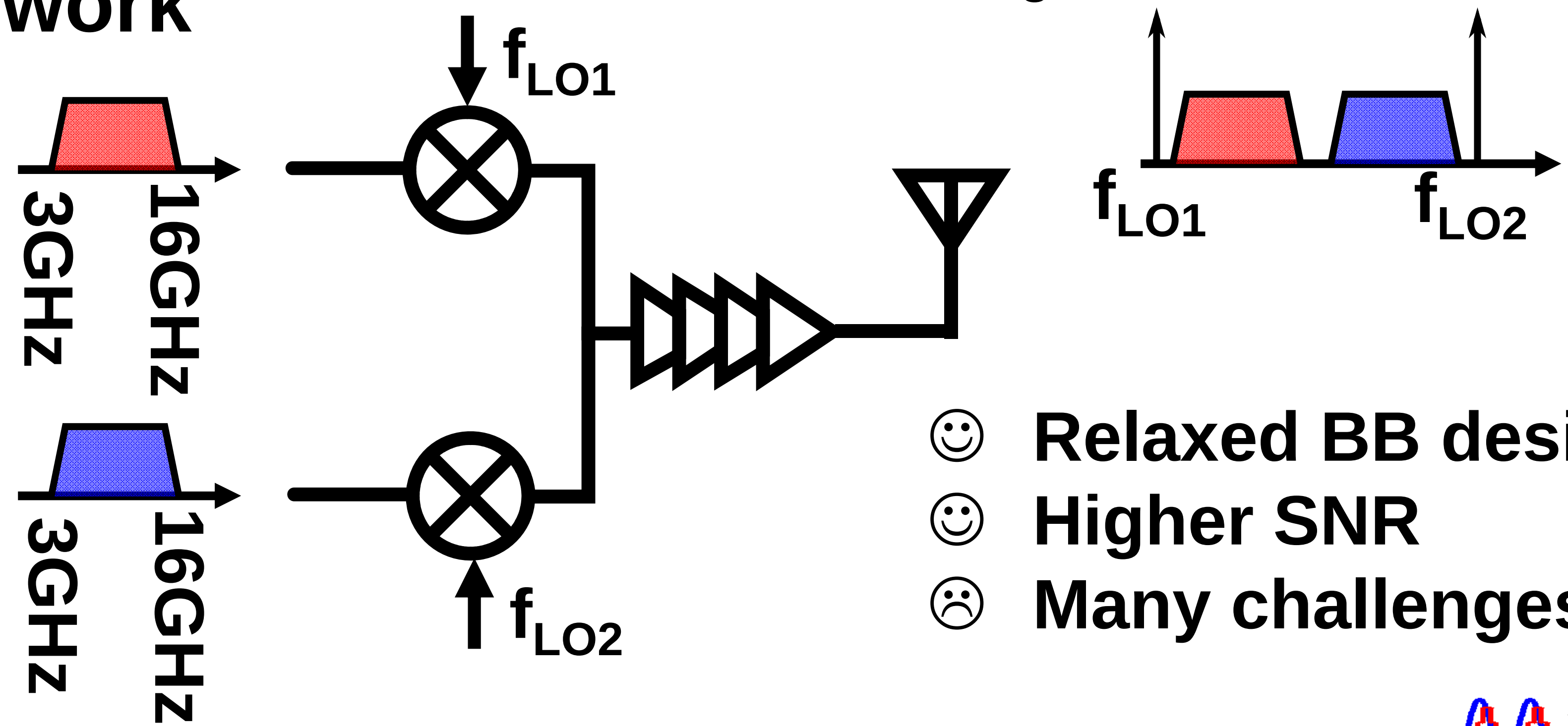
Challenge for Frequency Interleave (FI)

Conventional



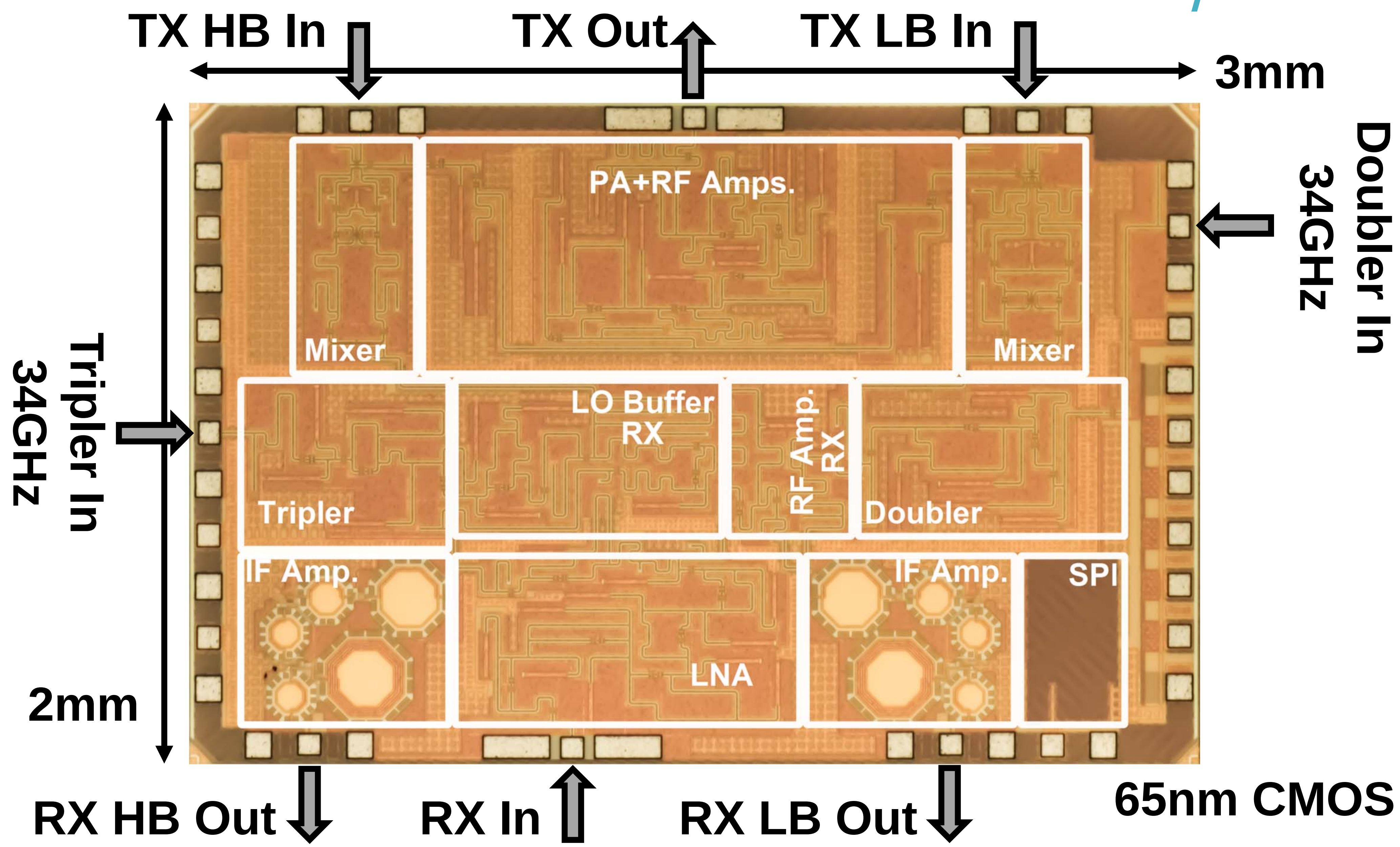
This work

ISSCC 2016, K. K. Tokgoz, K. Okada, A, Matsuzawa



- ☺ Relaxed BB design
- ☺ Higher SNR
- ☹ Many challenges

Die Photo of W-Band TRX



65nm CMOS

Comparison Table

Our group ([4], [8], This work)

Reference	[5, 6]	[7]	[4]	[8]	This work
Integration	TX, RX	TX, RX	TX, RX	TX, RX	TX, RX
Frequency [GHz]	240	155	57-66	57-66	68-102
Data Rate	16Gb/s (QPSK)	20Gb/s (QPSK)	28.16Gb/s (16QAM)	42.2Gb/s (64QAM)	56Gb/s (16QAM)
TRX Architecture	TX: Heterodyne RX: Direct Conversion	Hetero-dyne	Direct Conversion	Direct Conversion +Frequency Interleave	Heterodyne+ Frequency Interleave
Technology	65nm CMOS	45nm SOI	65nm CMOS	65nm CMOS	65nm CMOS
Power Cons. [mW]	TX: 220 RX: 260	TRX: 345	TX: 251 RX: 220	TX: 544 RX: 432	TX: 260 RX: 300

[4] K. Okada, *et al*., ISSCC2014 [5] S. Kang, *et al*., RFIC2014 [6] S.V. Thyagarajan, *et al*., RFIC2014
[7] Y. Yang, *et al*., RFIC2014 [8] R. Wu, *et al*., ISSCC2016.13.6

High data-rate circuit design

High data rate techniques

Wider bandwidth and higher SNR are required to attain higher data rate

Shannon's theory

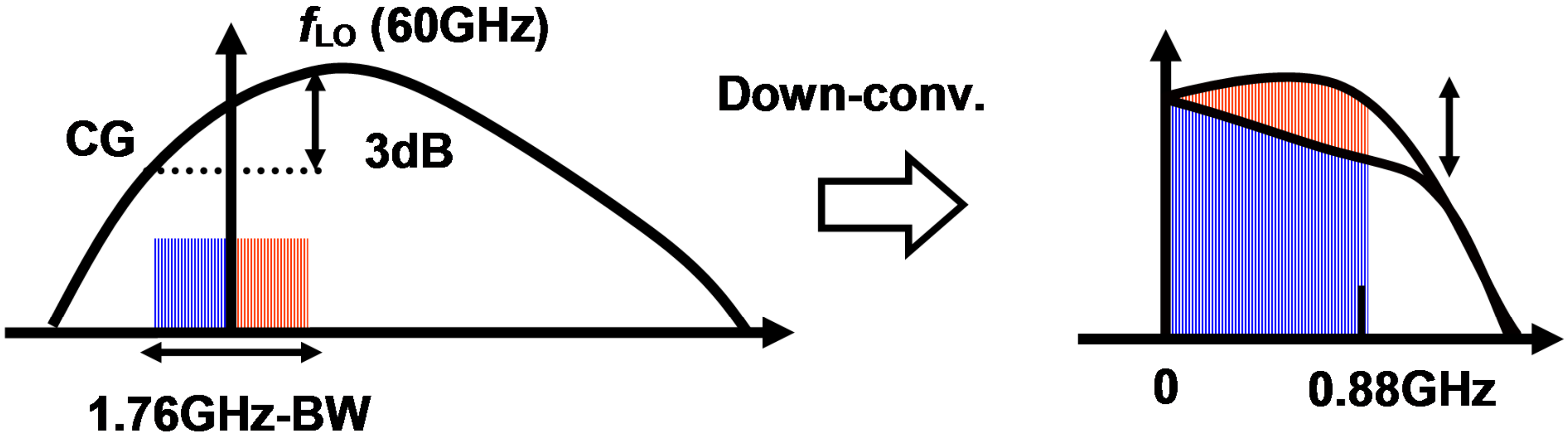
$$D_{rate} = BW \log_2\left(1 + \frac{S}{N}\right)$$

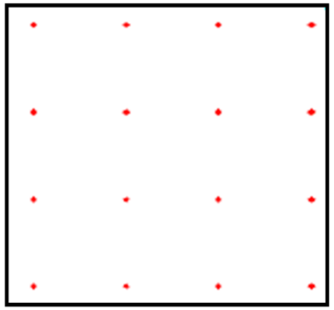
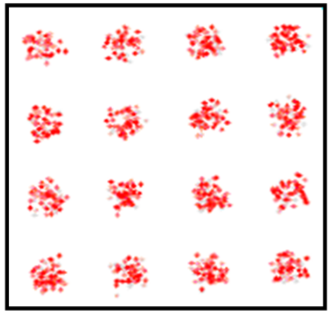
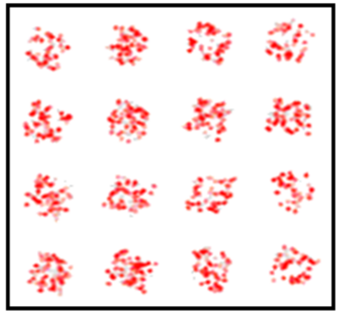
Wider bandwidth
- Multi-cascaded amplifier
- Passive mixer circuit
- Frequency interleaving

Higher SNR
- Injection locked I/Q oscillator
- 7 bit ADC

Effect of the gain flatness

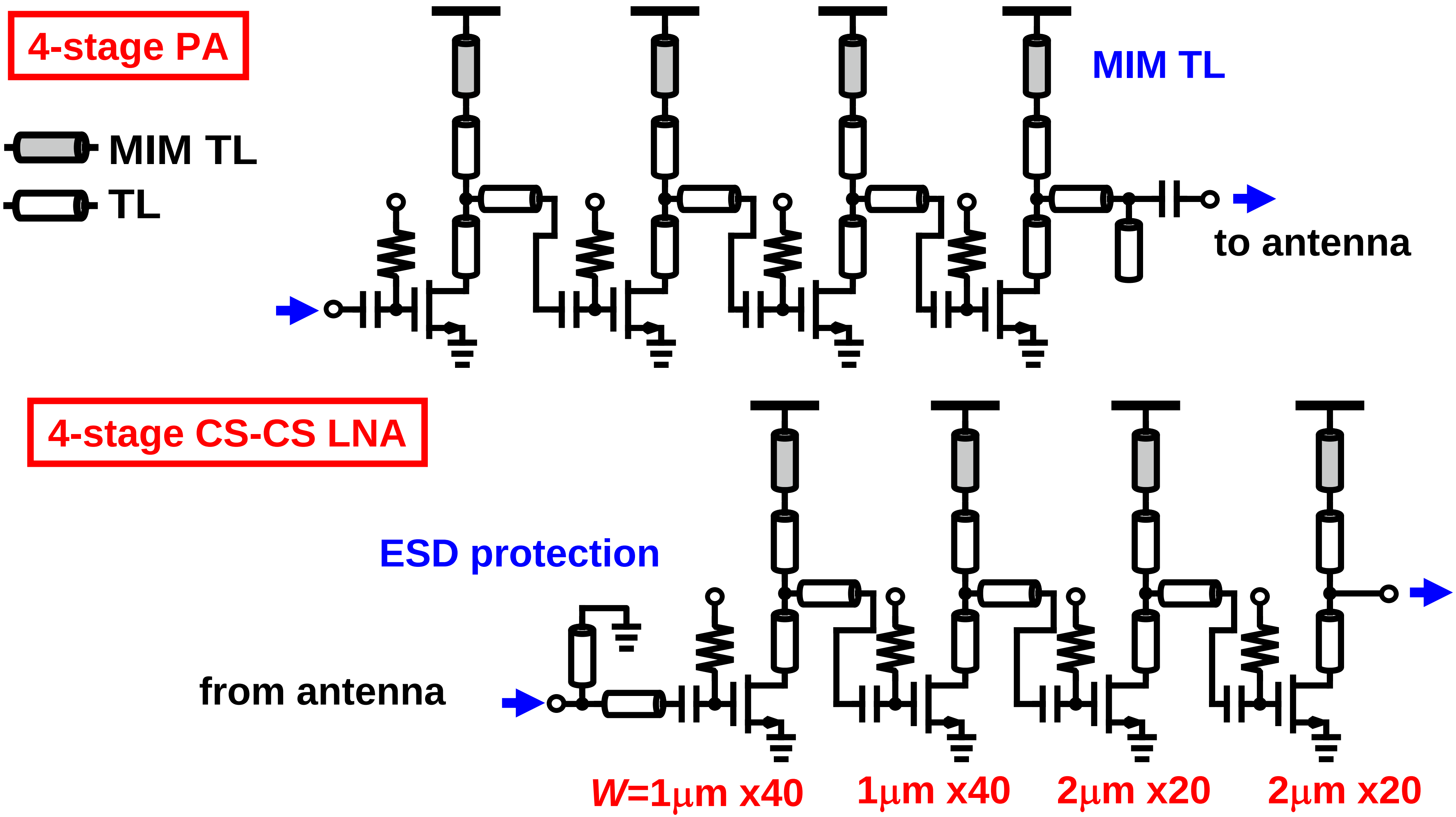
Poor gain flatness makes ISI (Inter Symbol Interference) due to different gain for plus frequency and minus frequency.



Gain Flatness	0dB	2dB	3dB
BER	~0	1.3e-5	3e-3
Constellation			

Multi-cascaded RF amplifiers

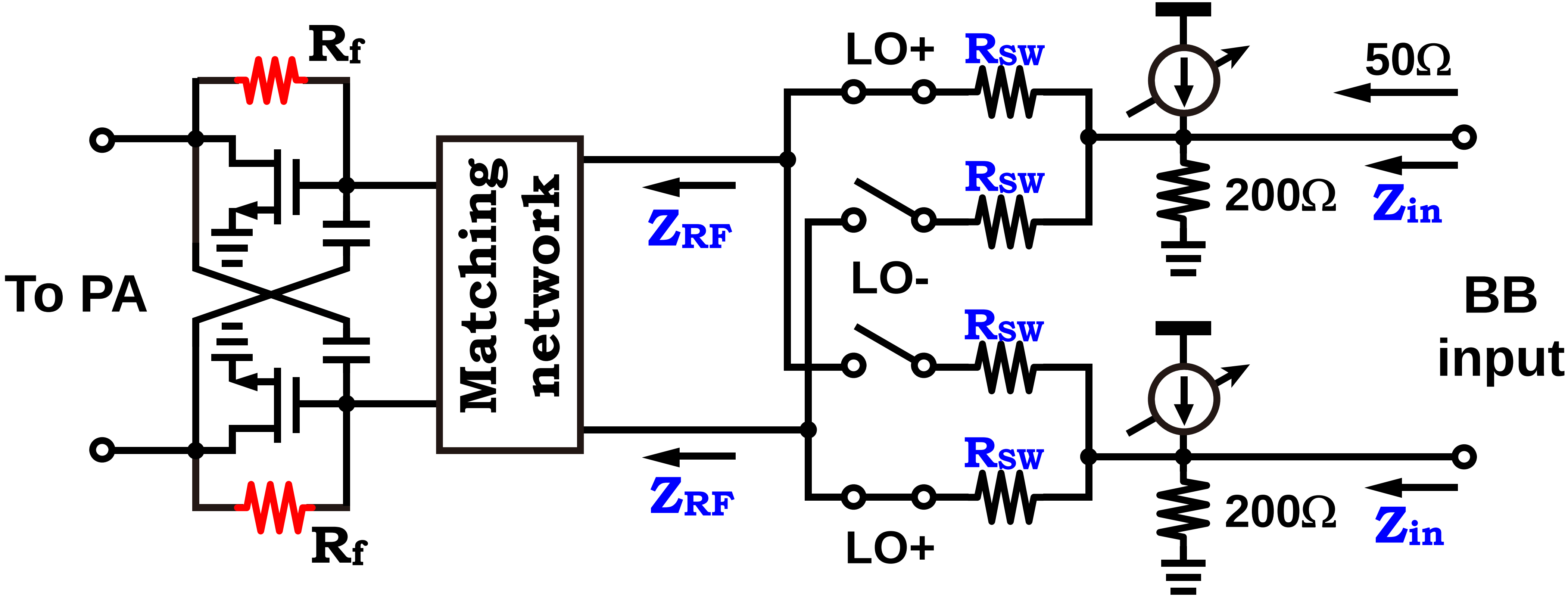
Multi-cascaded RF amplifier can increase the gain flatness due to the distributed resonant frequencies.



Mixer circuit in TX

Passive mixer with resistive feedback RF amplifier can realize Widely flat impedance, rather than LC impedance matching method.

$$Z_{in}(\omega) \approx 200\Omega // \left\{ R_{SW} + \frac{8}{\pi^2} \mathrm{Re}\left[Z_{RF}(\omega_{LO}) \right] \right\}$$



Measured gain of TX circuit

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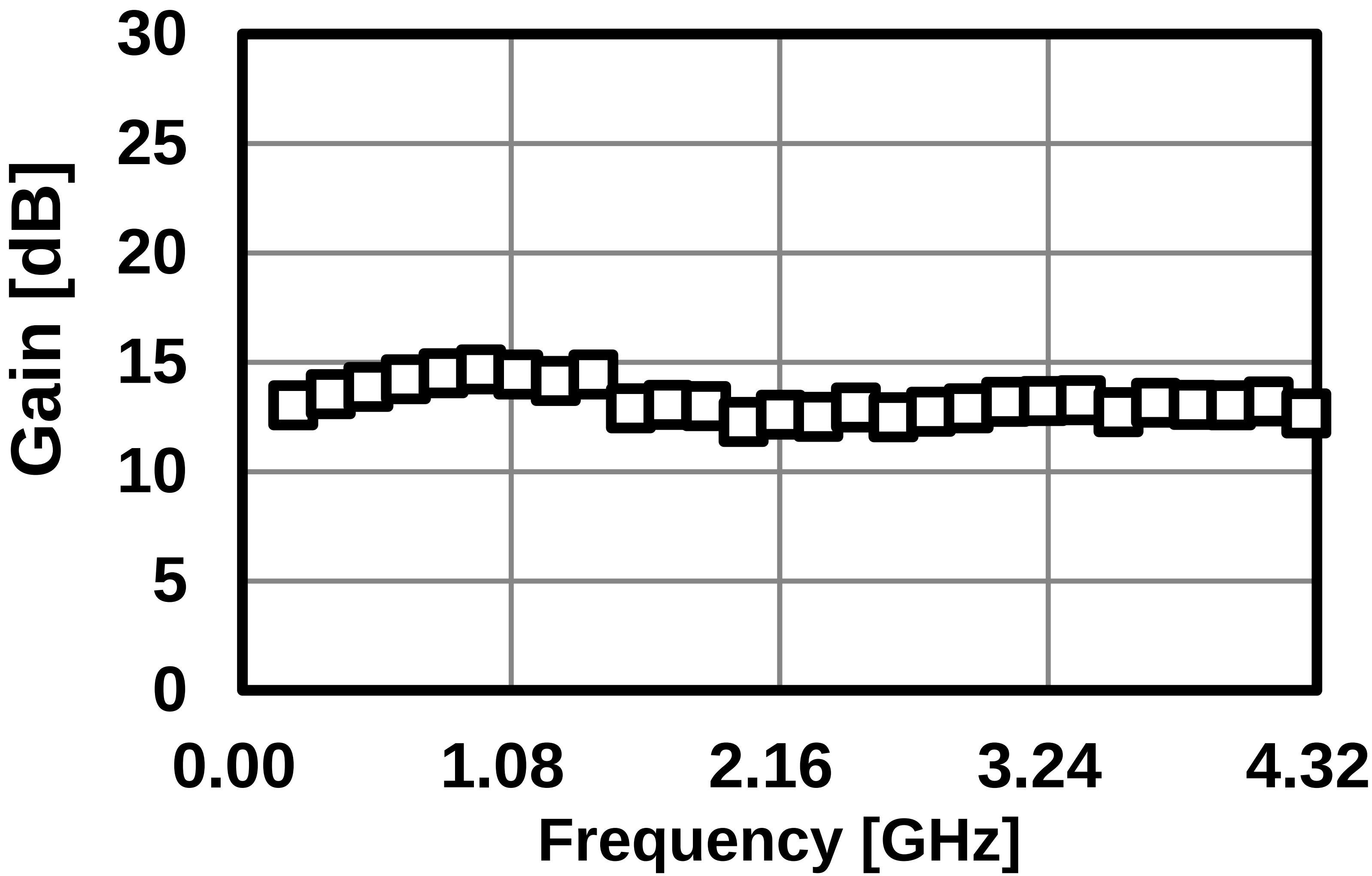
The gain flatness of 2 dB is attained for the band width of 4 GHz.



Required phase noise of IQ-VCO for 16QAM

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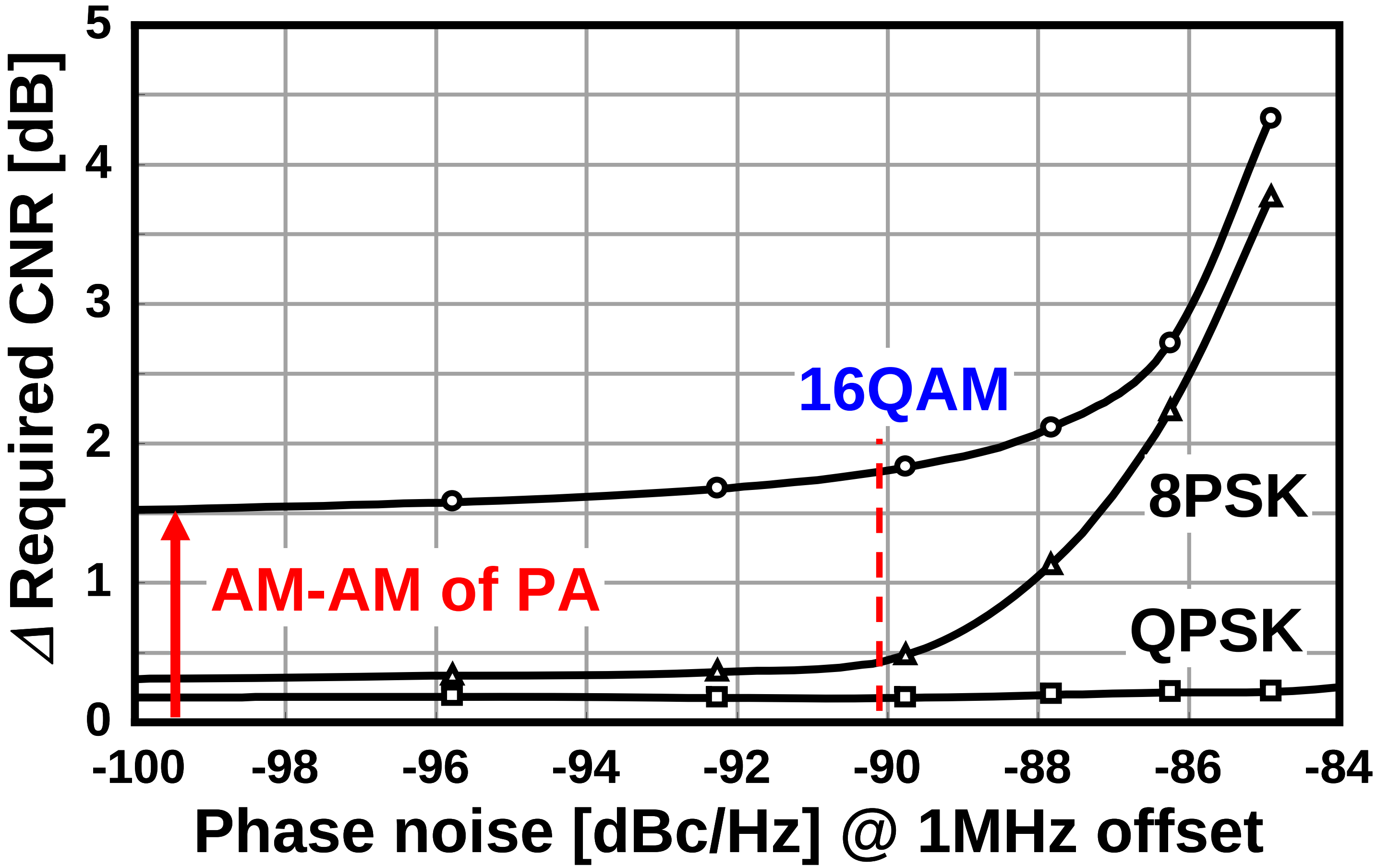
A phase noise of LT. -90dBc/Hz@1MHz is required for 16QAM systems

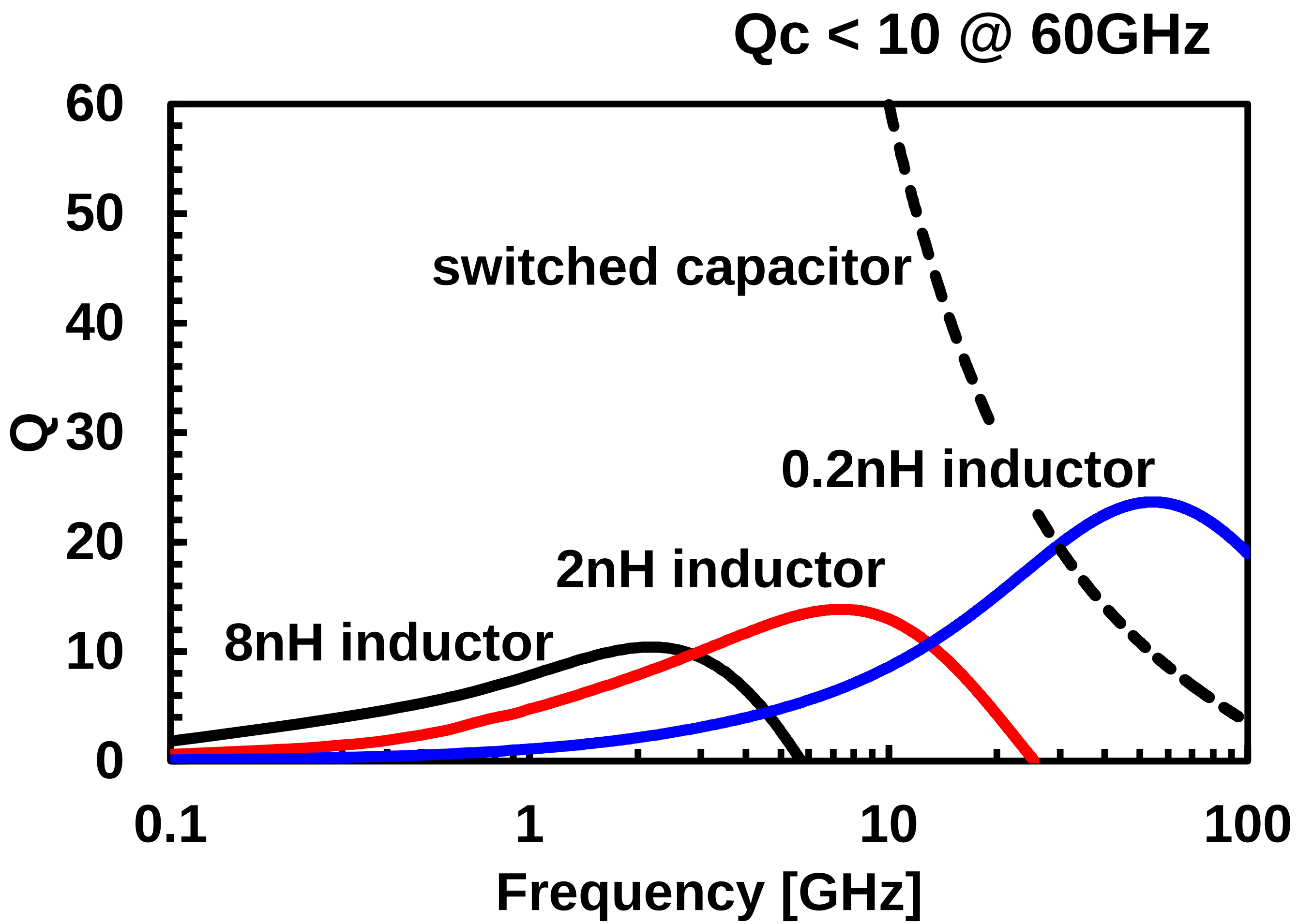
A reported phase noise of 60GHz IQ VCO is -76dBc/Hz @1MHz at most

K. Scheir, et al., ISSCC, pp. 494-495,Feb. 2009.



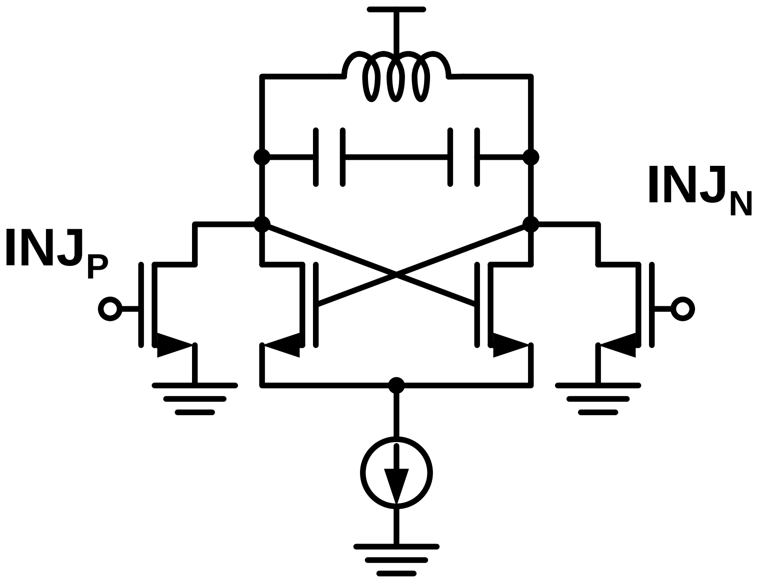
Q of inductors and capacitor

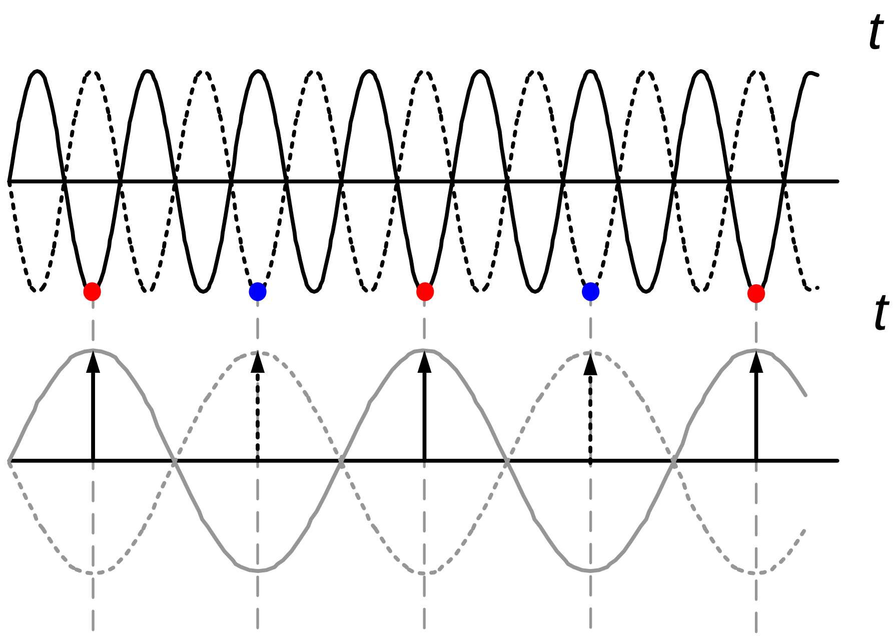
Q of capacitor is rapidly degraded with frequency.
Q of Less than 10 at 60 GHz at most.
→ Low phase noise 60 GHz VCO is hard to be realized.



Injection locking technique

Injection locking technique is a very important circuit technique for high frequency signal generation and frequency divider.
Phase noise of the oscillator is mandated by the injection.





Phase noise $$PN_{\mathrm{ILO}} = PN_{\mathrm{INJ}} + 20\log(N)$$ N: Multiple number

9.5dB @ N=3

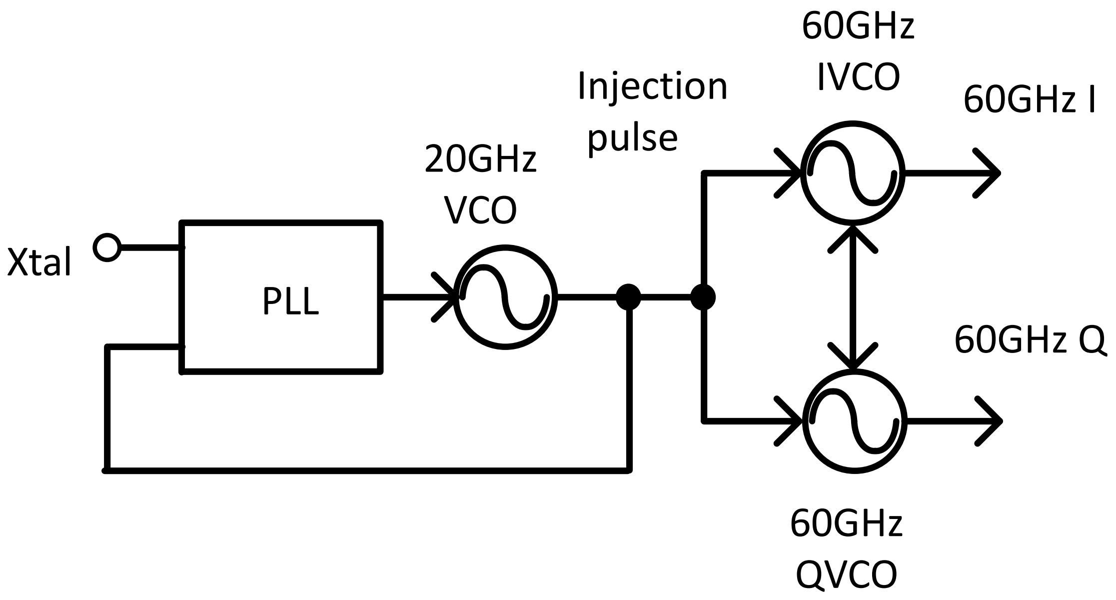
Locking frequency range $$f_L \approx \frac{f_o}{2Q} \cdot \frac{I_{inj}}{I_{OSC}}$$

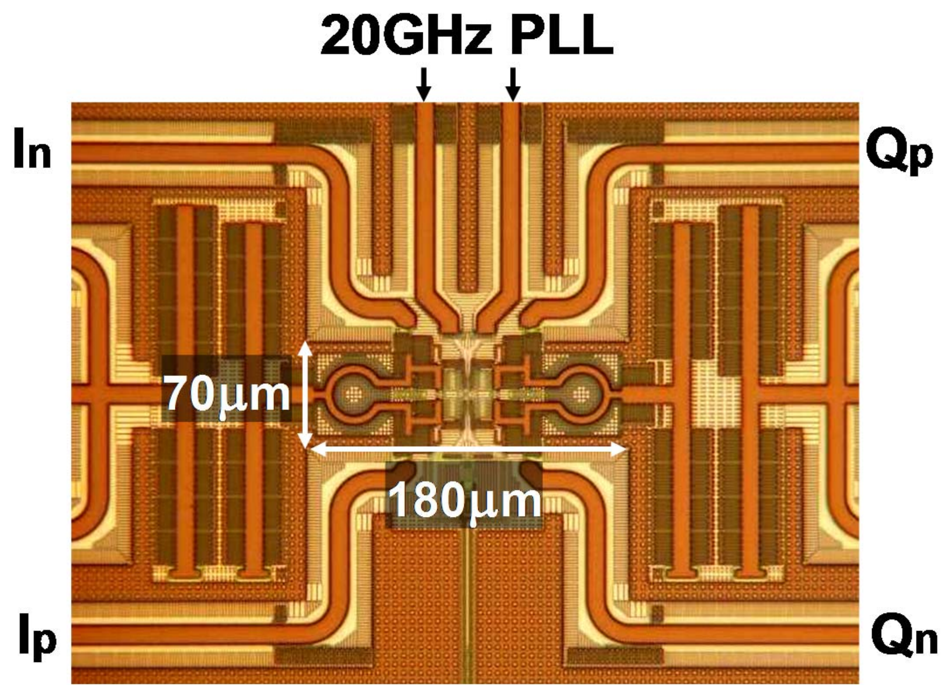
Injection locked 60GHz I/Q VCO

Developed the injection locked 60 GHz quadrature VCO

The 60 GHz quadrature VCO is injected by 20 GHz PLL

$$PN_{OSC}(dB) = PN_{INJ}(dB) + 20\log M$$





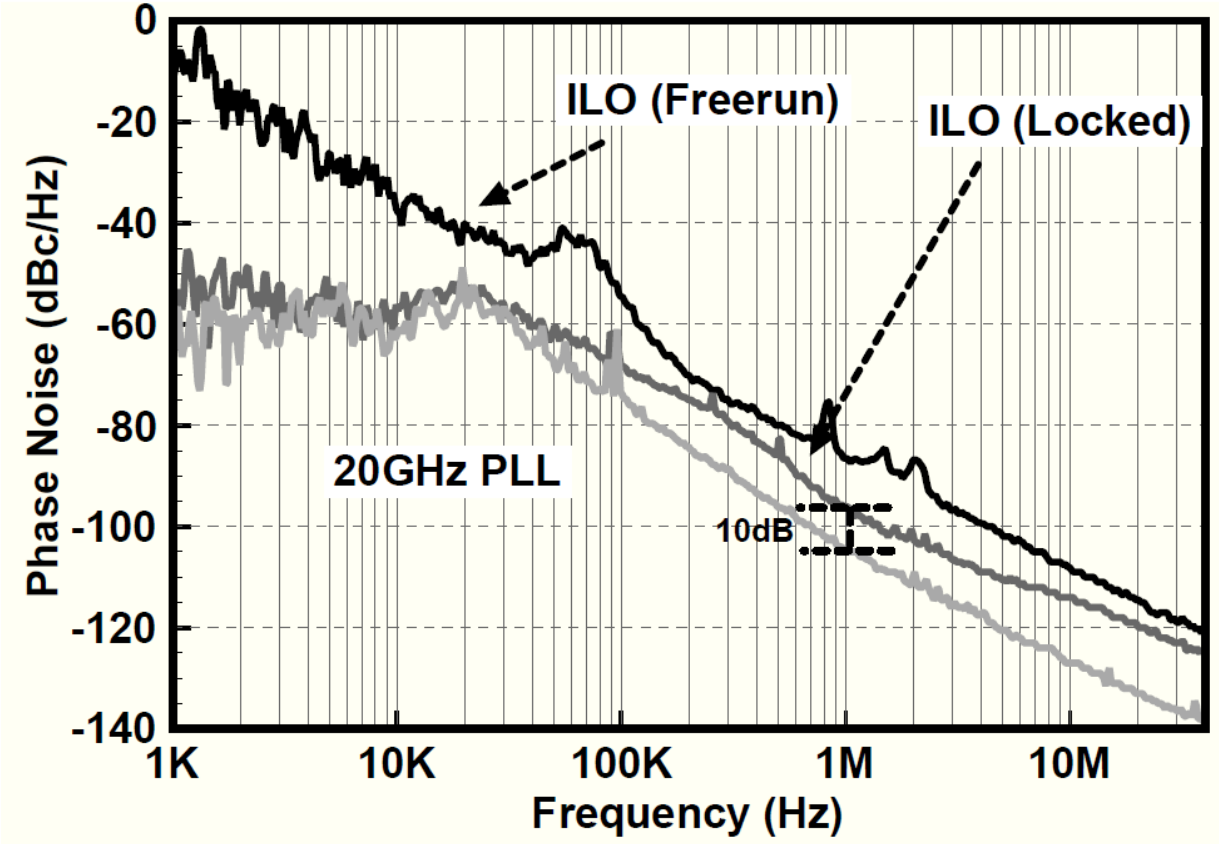
A. Musa, K. Okada, A. Matsuzawa., in A-SSCC Dig. Tech. Papers, pp. 101–102, Nov. 2010.

Low phase noise can be realized

Quadrature injection locked 60GHz oscillator with 20GHz PLL
Low phase noise of -96dBc/Hz @1MHz. Previous one is -76dBc/Hz@1MHz

Best phase noise is achieved.

58-63GHz, -96dBc/Hz-1MHz offset



A. Musa, K. Okada, A. Matsuzawa., in A-SSCC Dig. Tech. Papers, pp. 101–102, Nov. 2010.

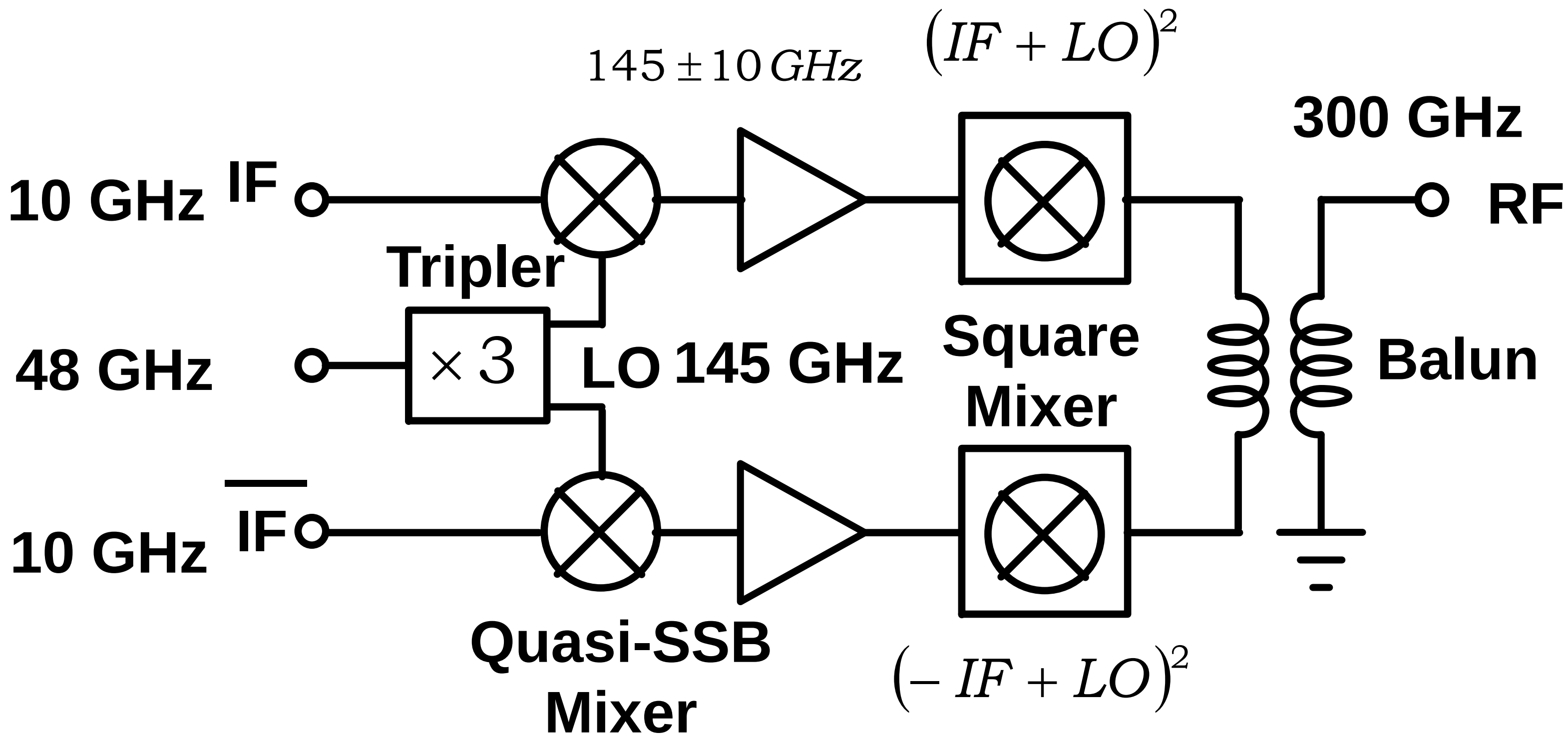
Conquer the f_{max} limit of CMOS

300 GHz Tx

Prof. Fujishima's group's work of Hiroshima Univ.

CMOS 300GHzTransmitter

It is almost impossible to amplify the 300 GHz signal by CMOS technology.
The 2nd step-up mixer is used and combine the signal in the balun.
To increase the RF power. The image suppression is needed.



K. Takano, et al., Hiroshima Univ., ISSCC 2017, S17.9

Performance comparison

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Comparable frequency with compound semiconductor devices.
Over 100 Gbps has been attained.

	[1]	[2]	[3]	[4]	[5]	This work	
Technology	250nm InP	35nm GaAs	35nm GaAs	0.13μm SiGe	40nm CMOS	40nm CMOS	
Freq. (GHz)	300	240	300	240	300	302	289–311
Modulation	QPSK	8PSK	QPSK	64QAM	16QAM	32QAM	128QAM
Pout (dBm)	–	−3.5	−4	7	−14.5	−5.5	
Pdc (W)	–	–	–	0.54	1.4	1.4	
Data rate (Gb/s)	50	96	64	1.02	28	105	24.64 x 6

[1] Song et al., TMTT, 2014.
[2] Boes et al., IRMMW-THz, 2014.
[3] Kallfass et al., IEICE Trans., 2015.
[4] Sarmah et al., TMTT, 2016.
[5] Takano et al., Electron. Lett., 2016.

K. Takano, et al., Hiroshima Univ., ISSCC 2017, S17.9

Future prospect of high data-rate wireless systems

Calculations for data rate of TRX

Calculate the data rate as function of career frequency and Tx power

Shannon's theory

$$D_{rate} = BW \log_2 (1 + SNR)$$

$$D_{rate} \approx BW \frac{\log_{10}(SNR)}{0.3} = BW \frac{SNR(dB)}{3}$$

Received signal

$$P_{RX}(dB) = P_{TX} - B_{OFF} + G_{AT} + G_{AR} - I_L - S_{LOSS}$$

Spatial loss

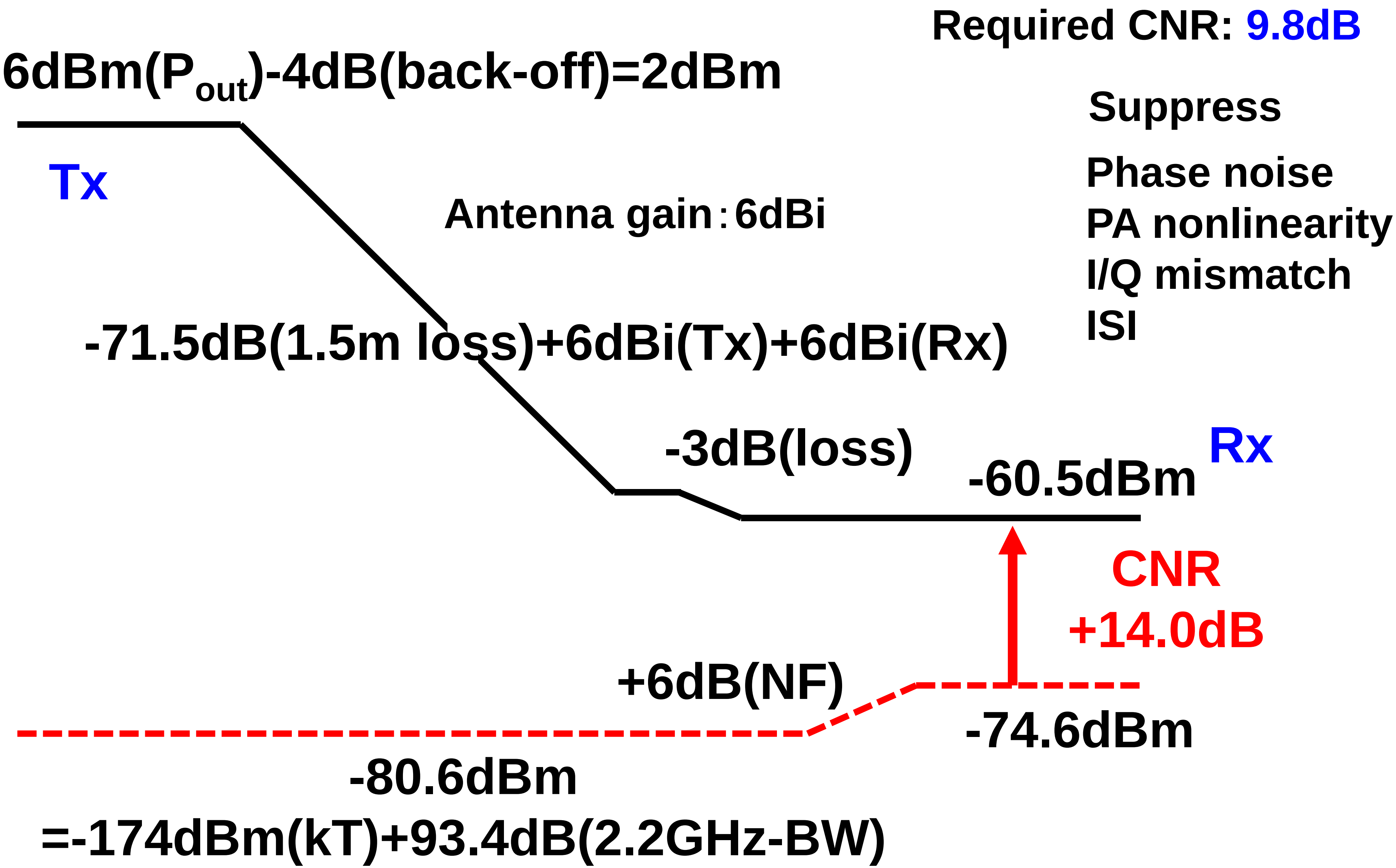
$$S_{LOSS} = -20\log\left(\frac{\lambda}{4\pi d}\right) = -20\log\left(\frac{c}{4\pi d f_c}\right) = 20\log\left(\frac{4\pi}{c} d f_c\right)$$

d: distance
f_c: career frequency

Noise

$$P_n(dBm) = -174 + 10\log BW + NF$$

60GHz Link budget (QPSK)



Estimated data rate

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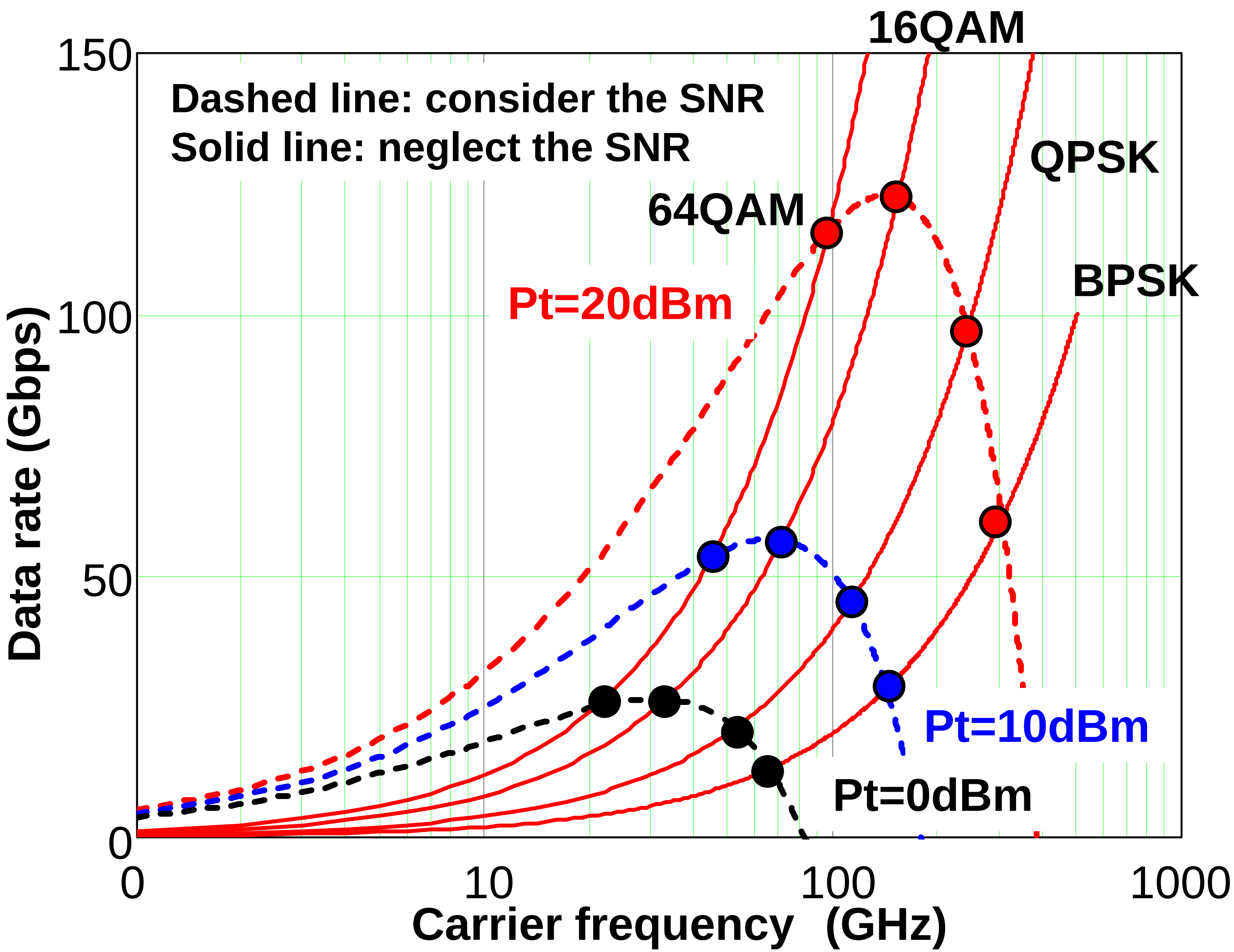
Higher data rate can be expected up to the certain frequency, however it is reduced after that frequency.
Higher power is required to increase the data rate.



Distance：1m
Antenna gain：6dBi
NF: 6dB
Back off： 4dB
Power loss： 3dB

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Future direction

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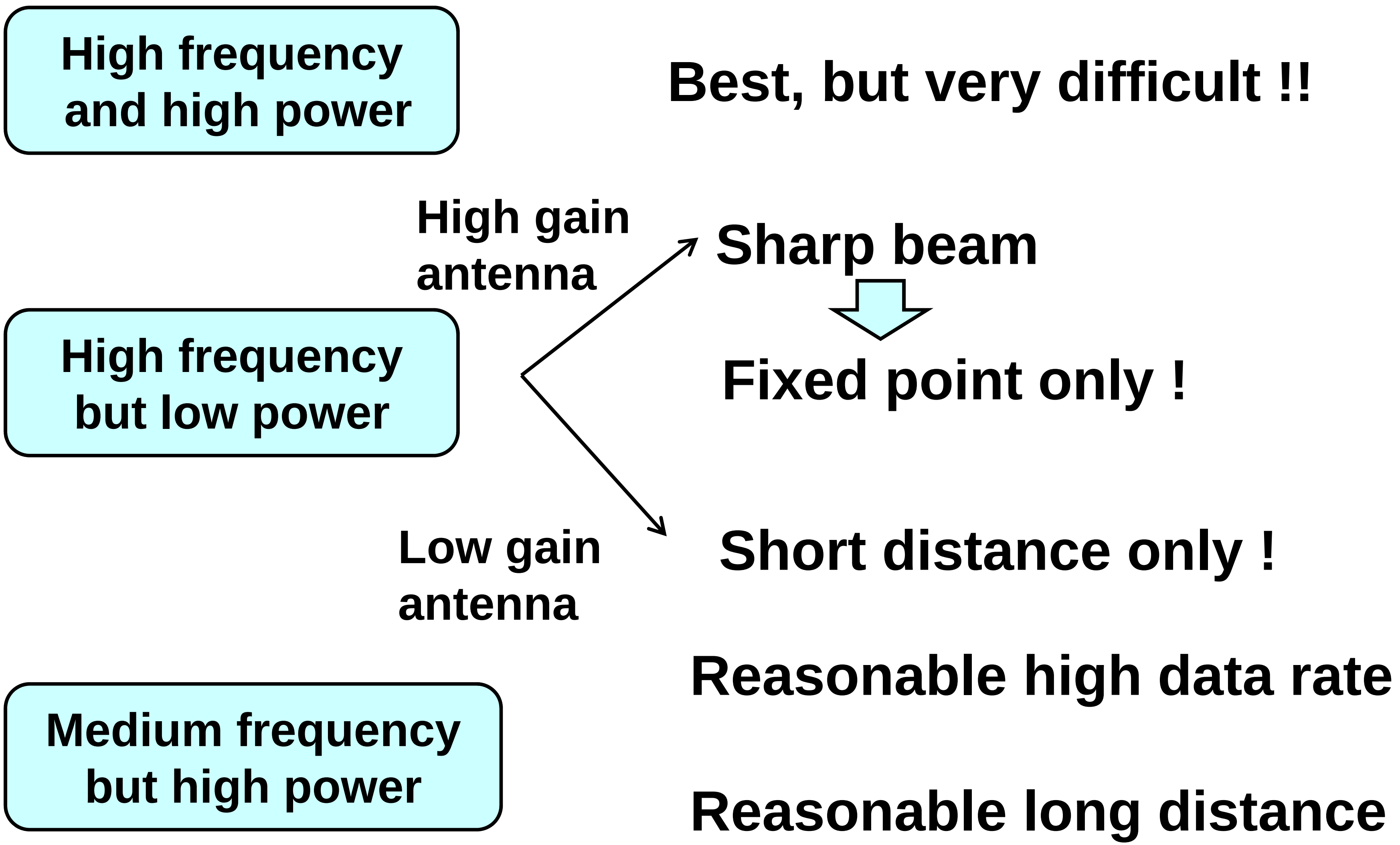
Future direction should be chosen by the usage model



Summary