

A Fully Synthesized Fractional-N IL-PLL Using Only Digital Library

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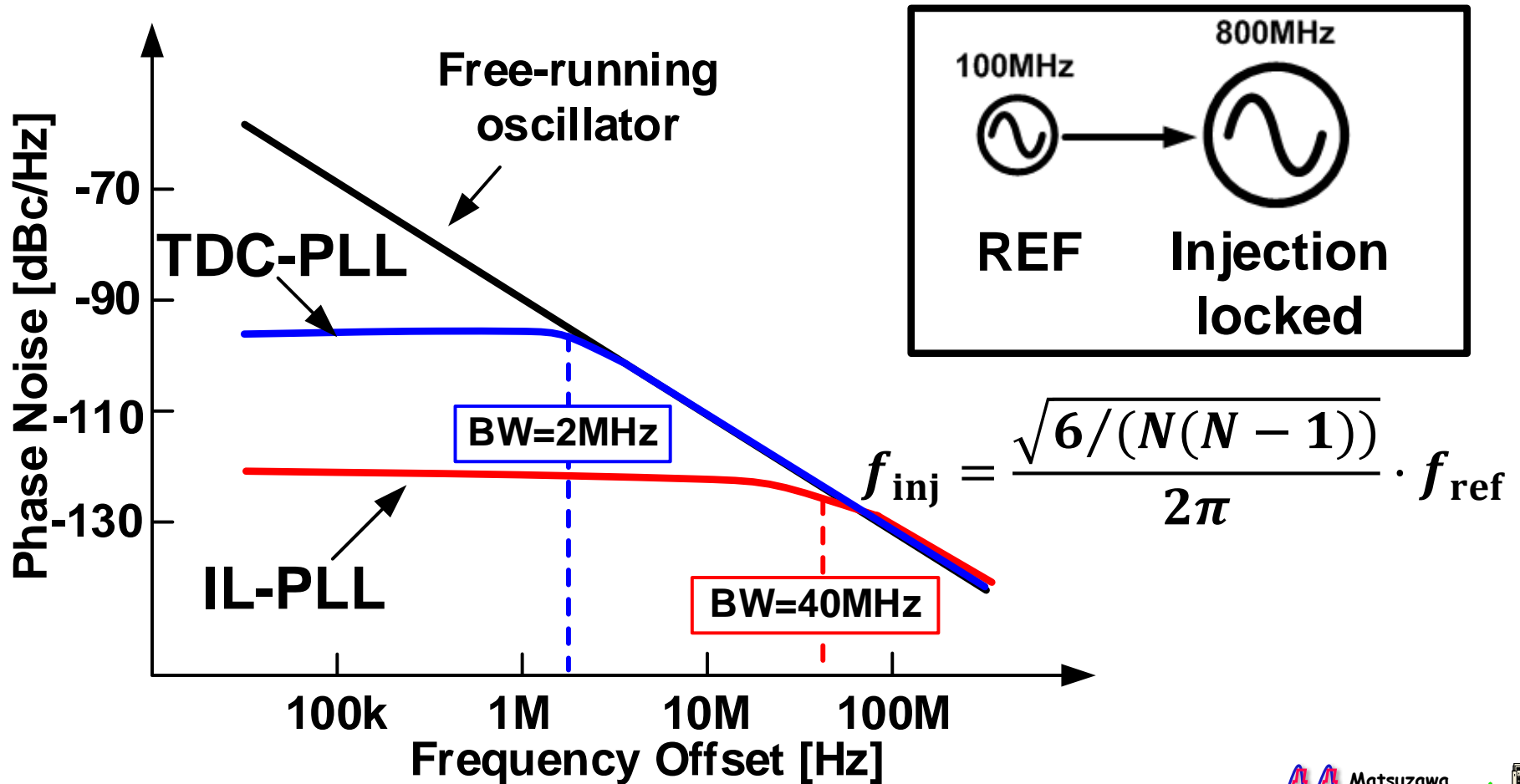
- **Motivation**
- **Concept of Injection Locking**
- **Fractional- N Implementations**
- **Performance Comparison**
- **Conclusion**

- **Why High Performance PLL**
 - Clock generation/distribution
- **Key Specifications for SoC Clocking**
 - Small area
 - Low power consumption
 - Low jitter
 - Insensitive over environment variations
 - Scalable with technology advancement

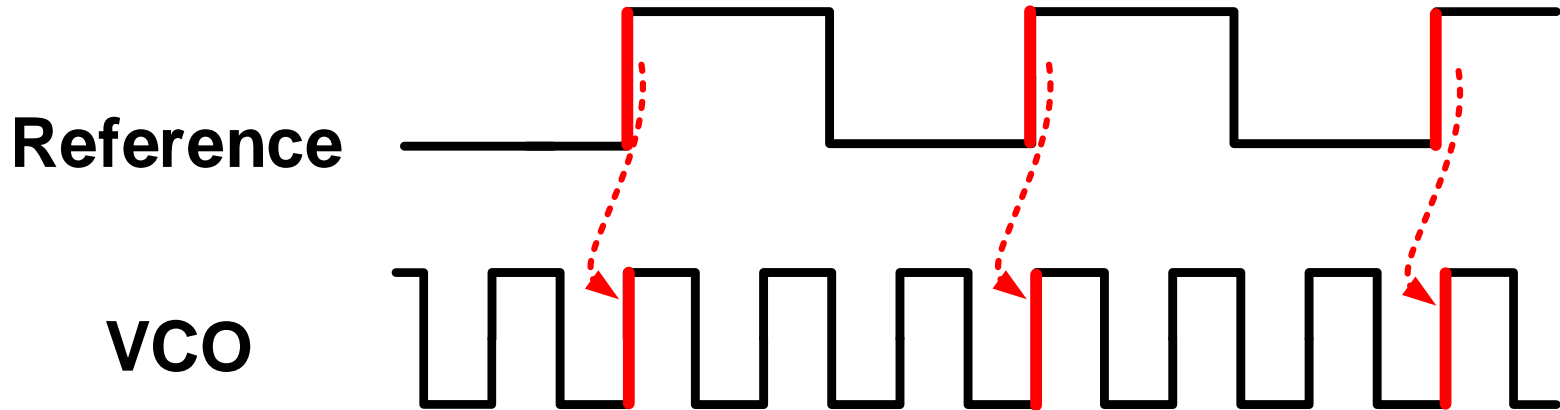
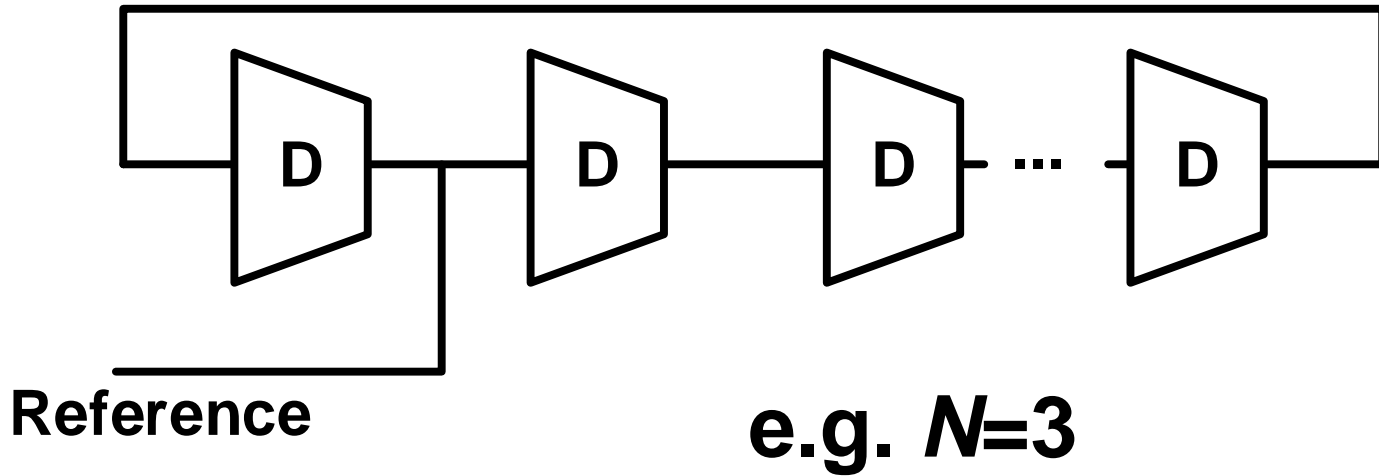
[1] W. Deng, *et al.*, ISSCC2014

Injection Locking Technique

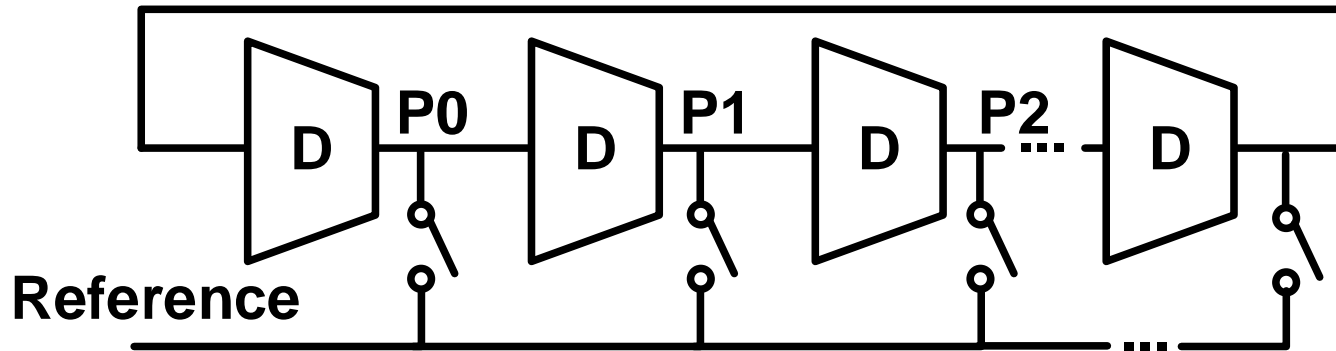
Jitter_{TDC-PLL} = 6.4ps Jitter_{IL-PLL} = 1.5ps



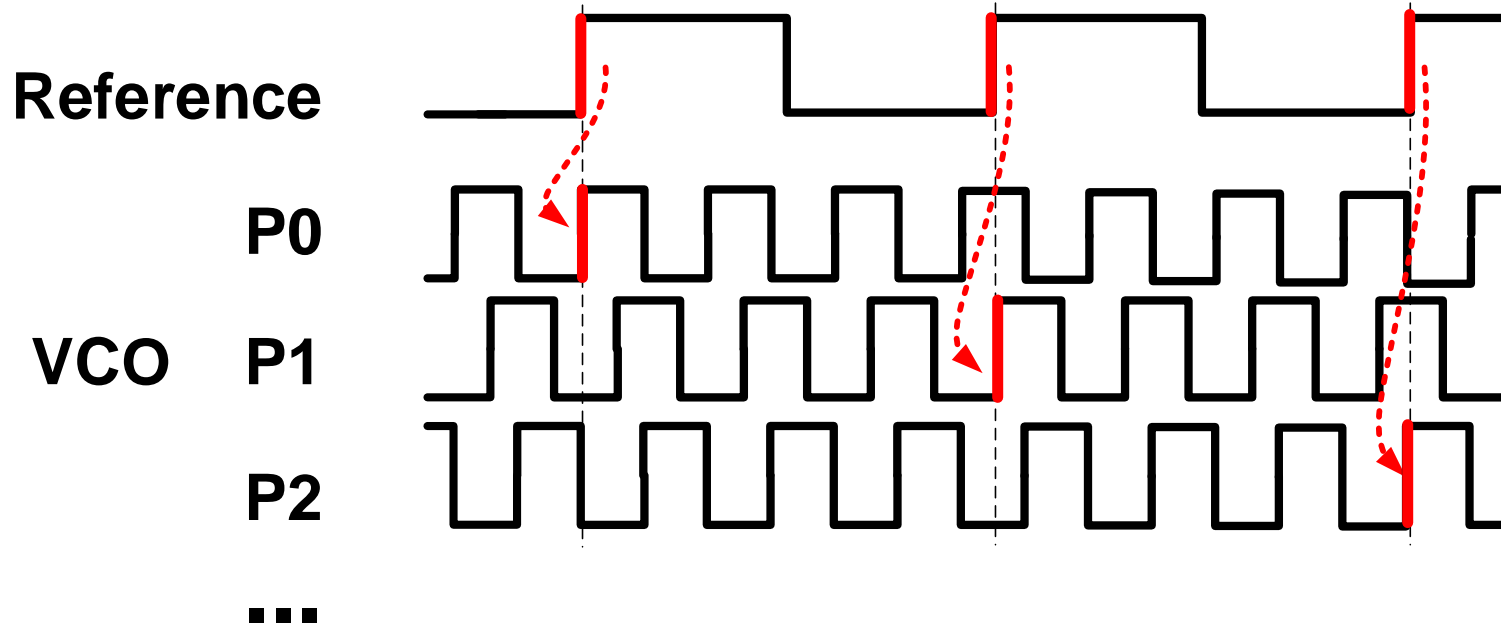
Integer- N Operation



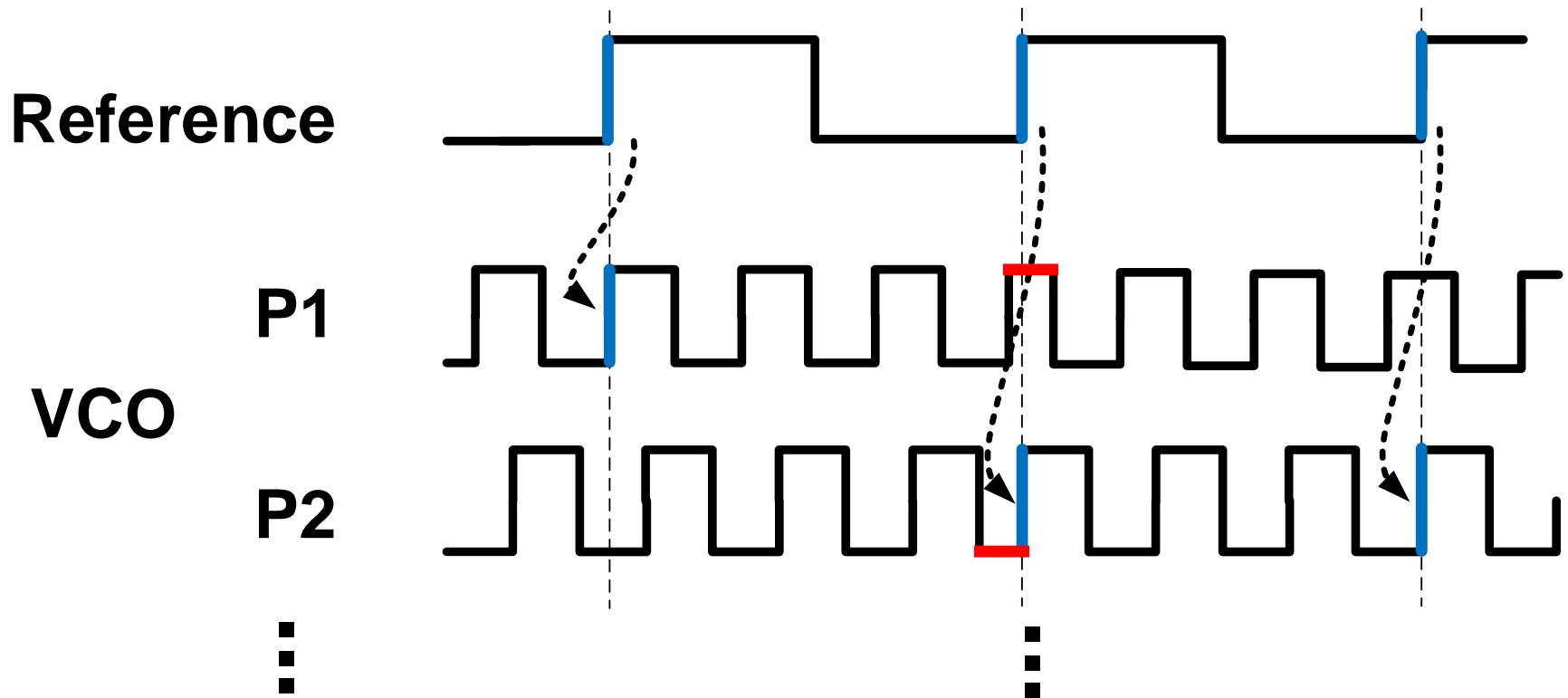
Sub-Integer-N Operation



e.g. $N=3+(1/M)$

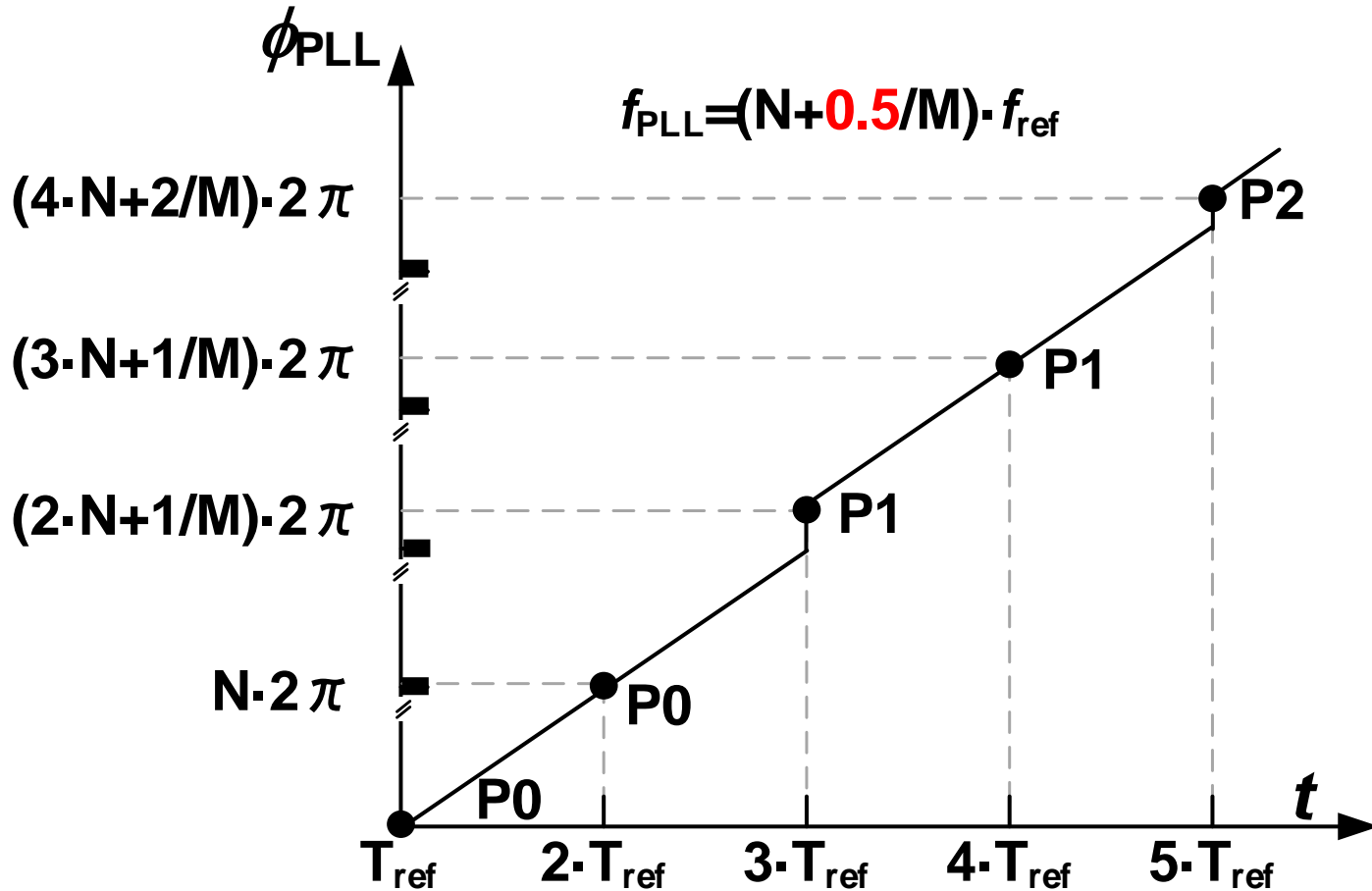


[P. Park, et al., ISSCC 2012]



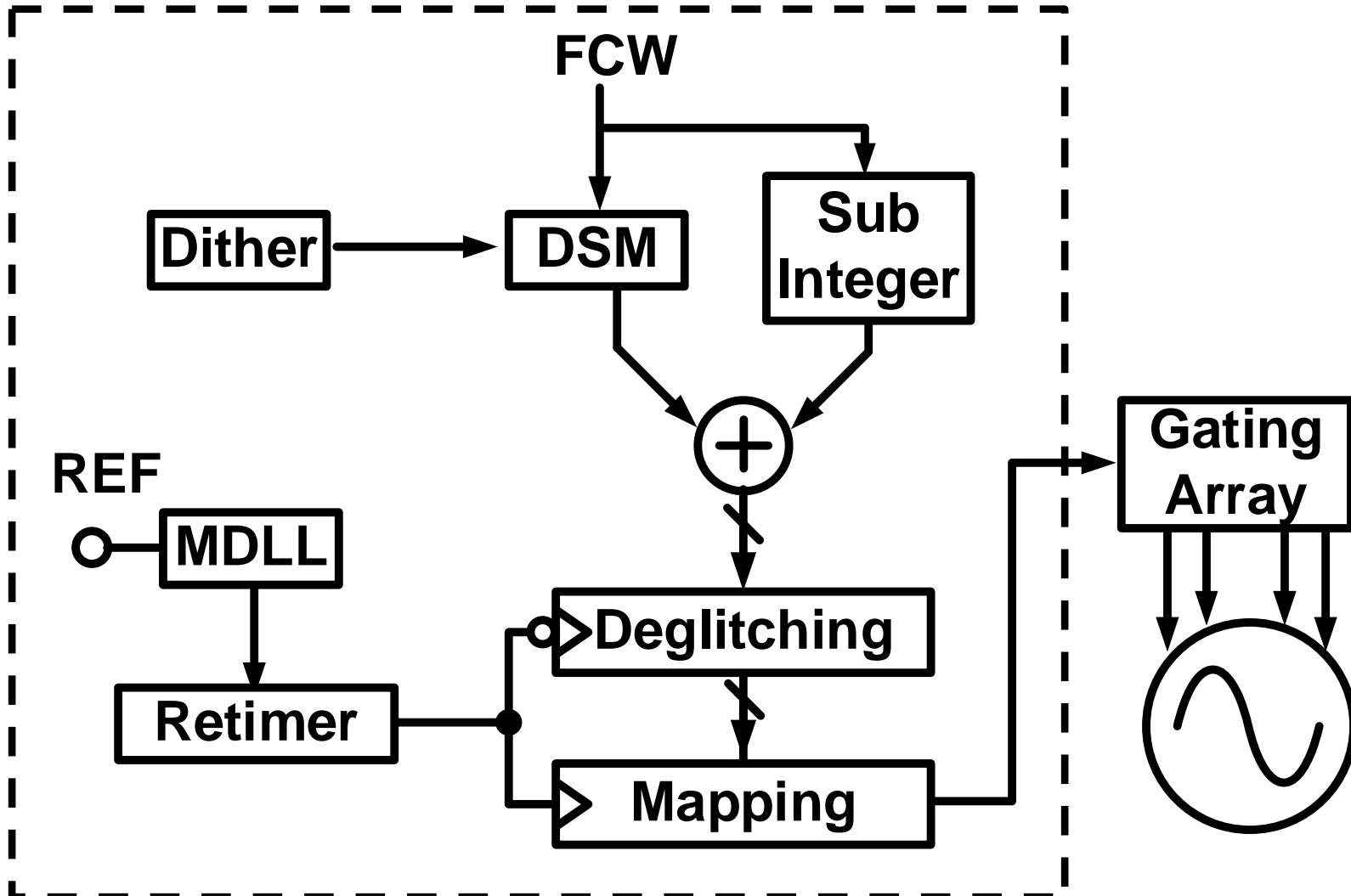
- Injection at the same phase two times

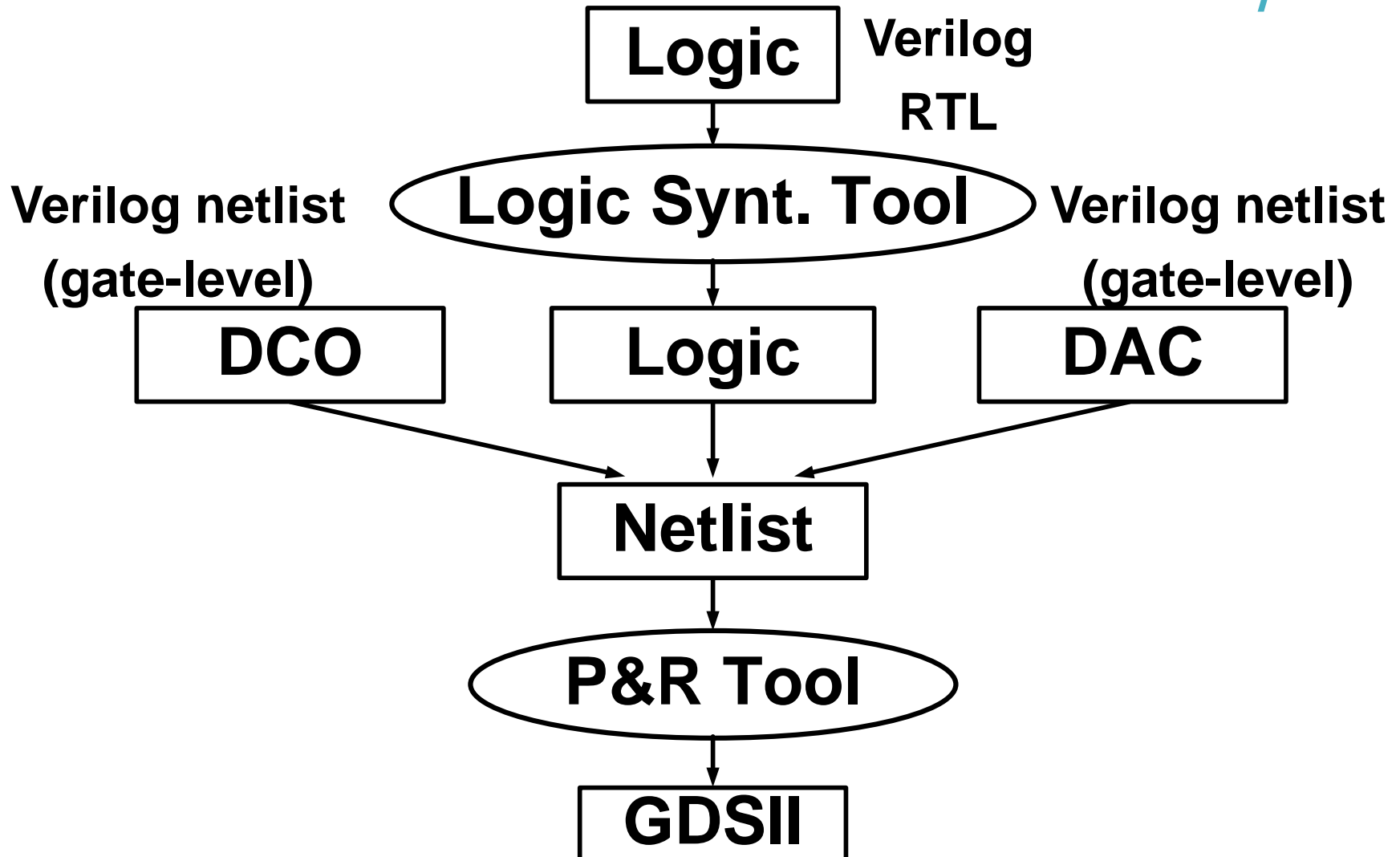
[2] W. Deng, *et al.*, ISSCC2015

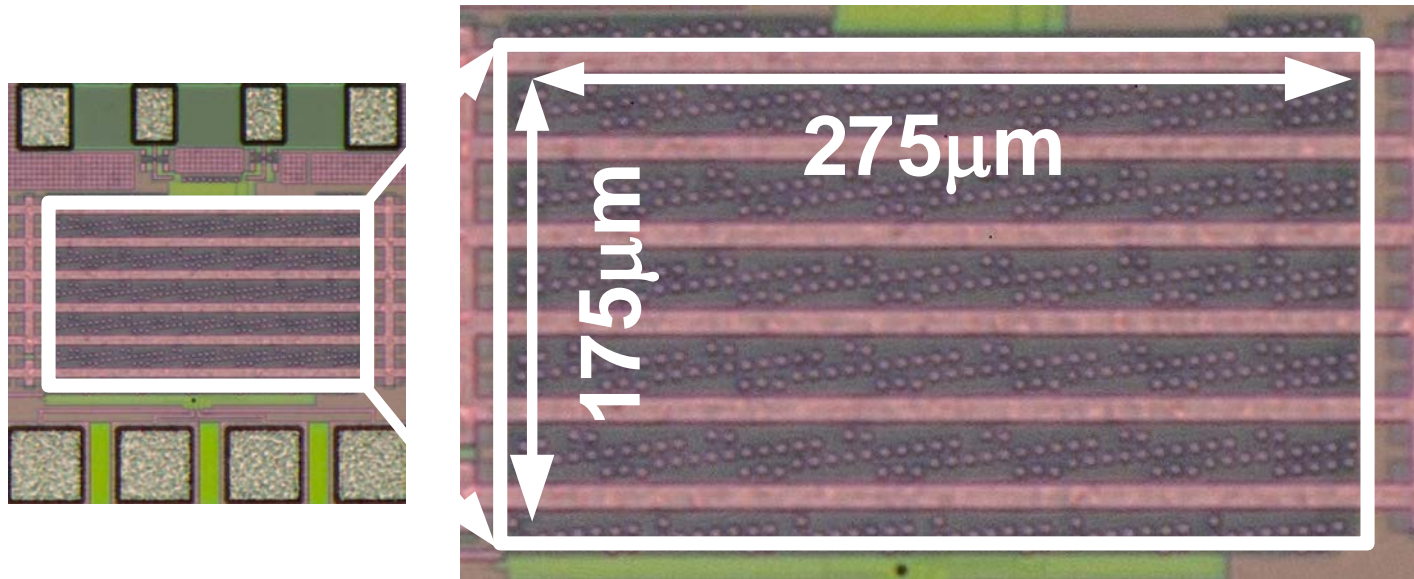


P0 → P0 → P1 → P1 → P2 → P2 → P3 ...

[2] W. Deng, et al., ISSCC2015







CMOS 65nm technology

	This work	[1]	[4]	[5]
CMOS	65nm	65nm	65nm	65nm
Topology	Soft Injection locking	Injection locking	DTC-based MDLL	Injection locking
Type	<u>Frac-N</u>	Int-N	Frac-N	<u>Sub-Int-N</u>
Frequency [GHz]	0.8-1.7	0.39-1.41	1.6-1.9	0.25-1.65
Power [mW]	3 @1.5222GHz	0.78 @0.9GHz	3 @1.7GHz	10.5 @0.58GHz
FoM [dB]	<u>-224.2</u>	-236.5	-232	<u>-221.9</u>
Synthesizable ?	Yes		No	

*FOM is calculated based on RMS jitter.

- **A fully synthesizable fractional- N IL-PLL is presented.**
- **Only digital library is used in the whole design.**

Thank you for your attention
Q & A