TOKYO TECH
Pursuing Excellence

An Automatic Place-and-Routed Two-Stage Fractional-*N* Injection-Locked PLL Using Soft Injection

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Synthesizable Analog Circuits

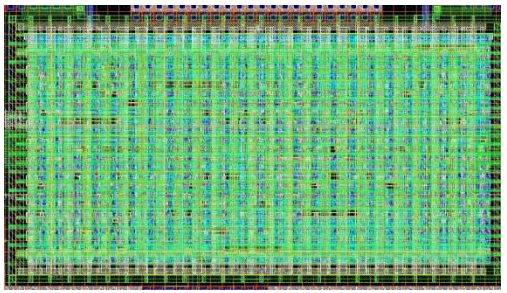
HDL

```
module PLL
(CLK, …, OUT)
…
endmodule
```

Digital design flow

e.g. Encounter, IC Complier, Design Compiler, PrimeTime, Commercial P&R tools…

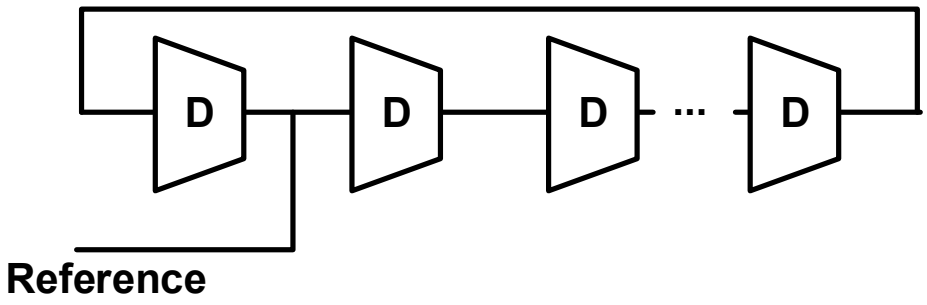
GDS



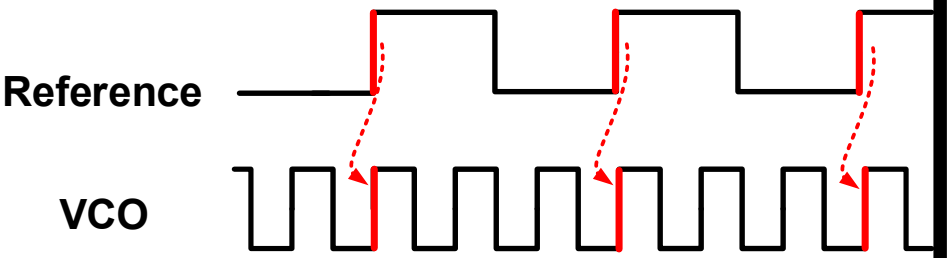
with a standard-cell library
without any custom-designed cells
without manual placement

[W. Deng, *et al.*, ISSCC 2014]

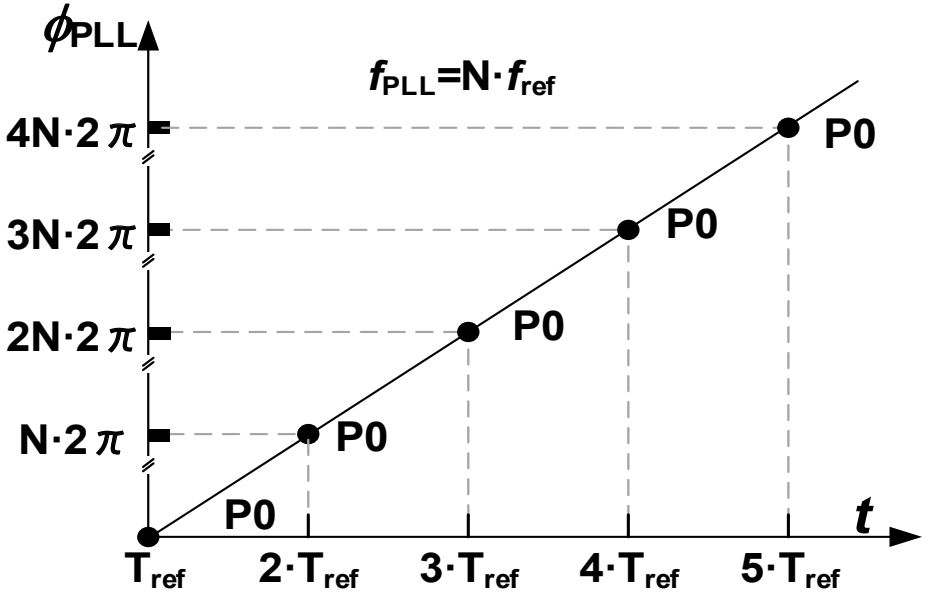
Integer-*N* IL-PLL Operation



e.g. *N*=3+(1/M)

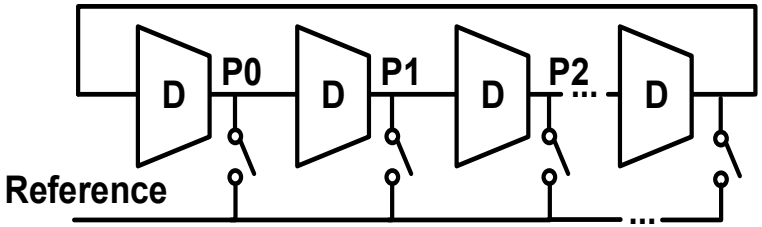


Phase Domain (Integer-*N*)

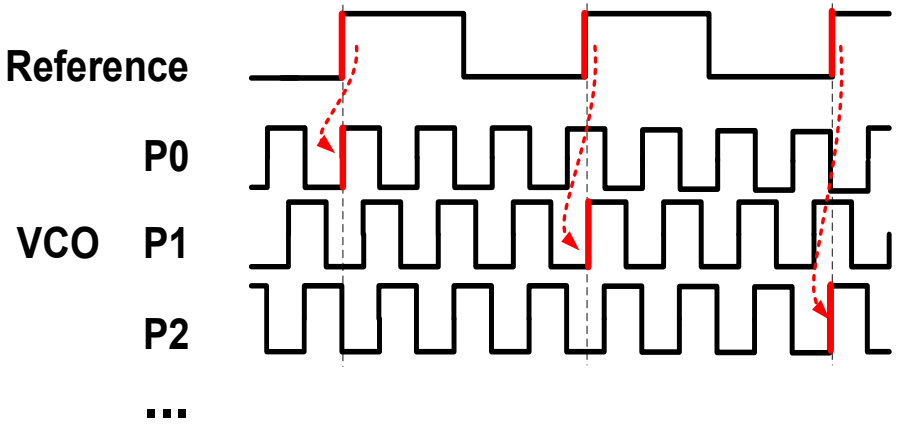


P0 → P0 → P0 → P0 → P0 → P0 …

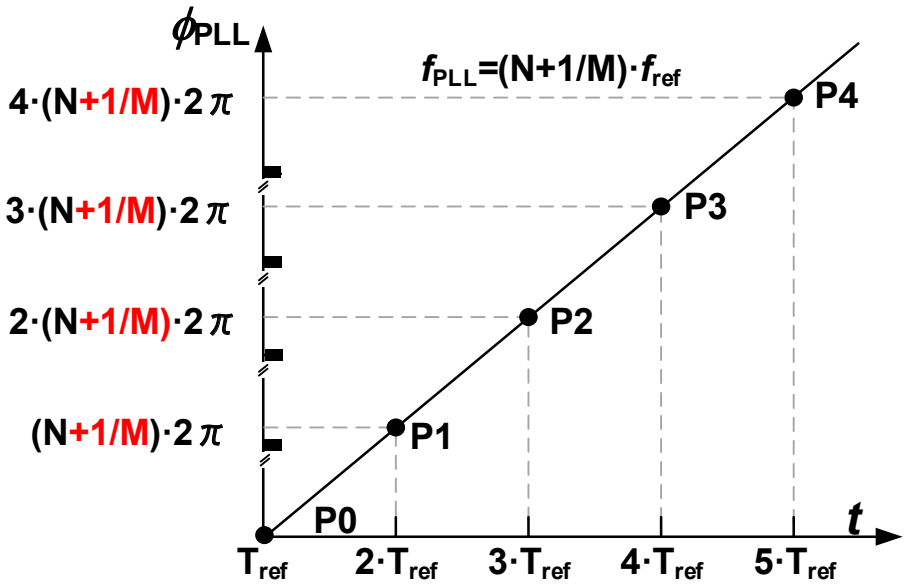
Sub-Integer-*N* IL-PLL Operation



e.g. *N*=3+(1/M)



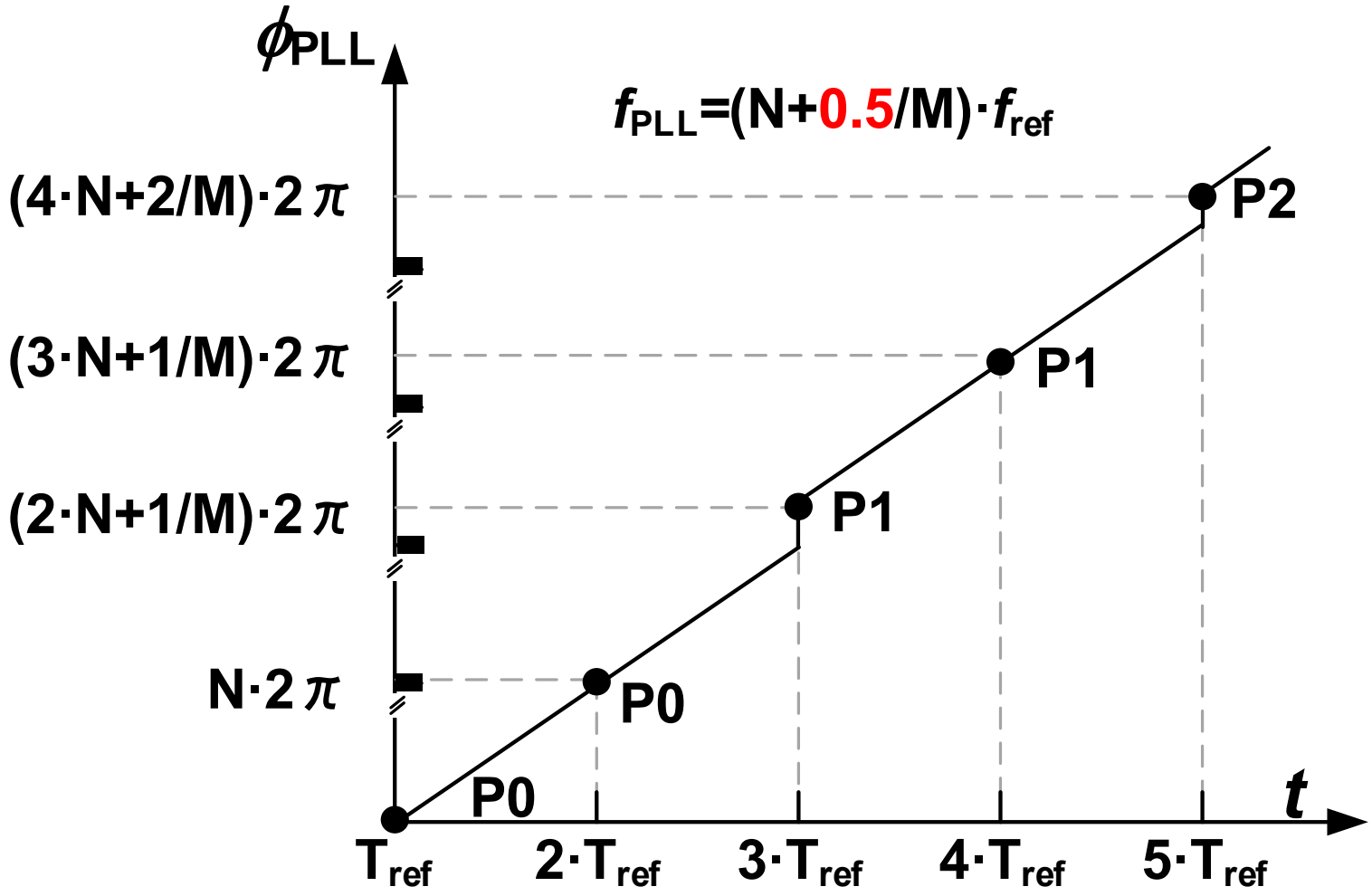
Phase Domain (Sub-Integer-*N*)



P0 → P1 → P2 → P3 → … → P0 → P1 …

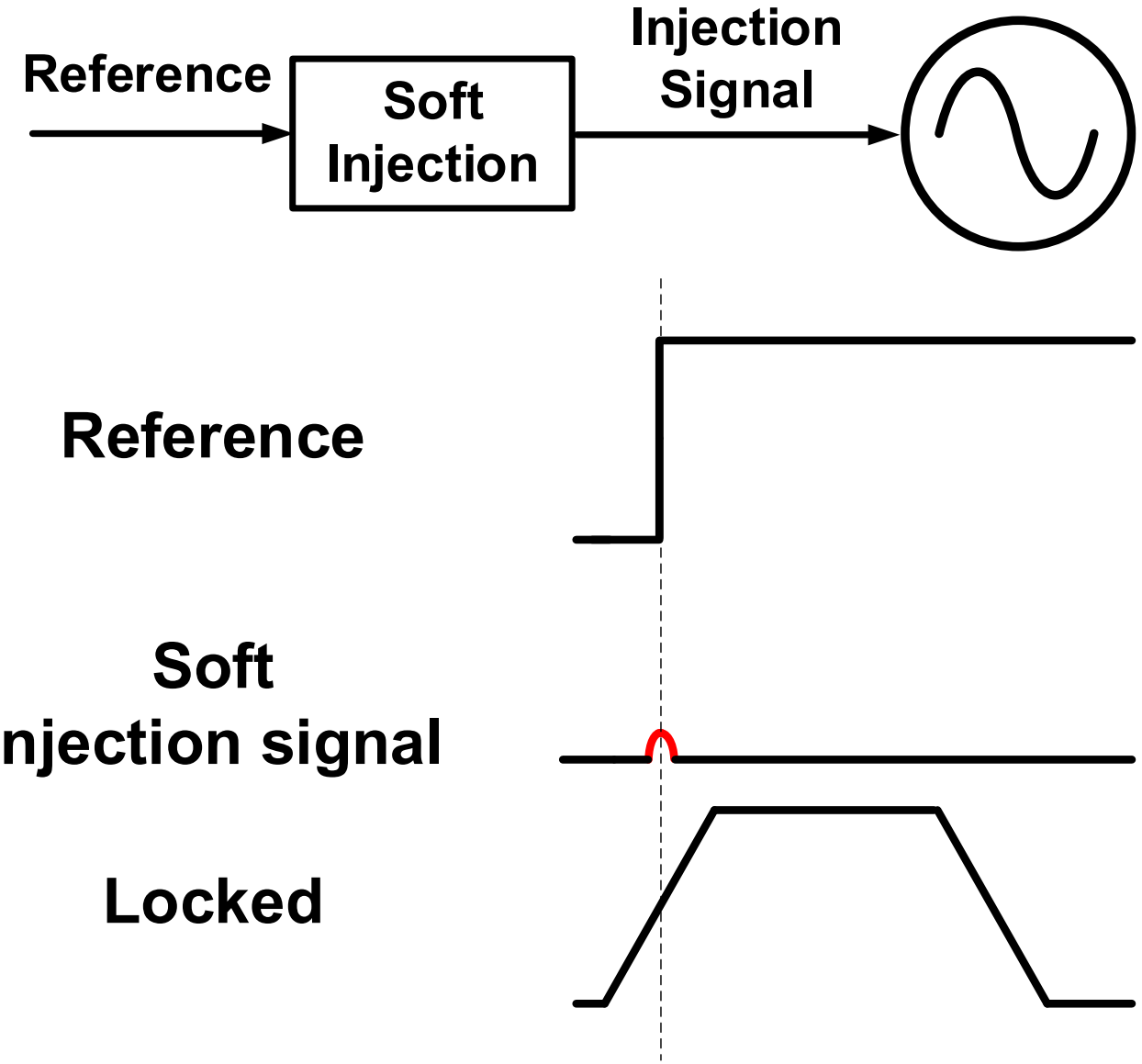
[P. Park, *et al.*, ISSCC 2012]

Phase Domain (Fractional-*N*)

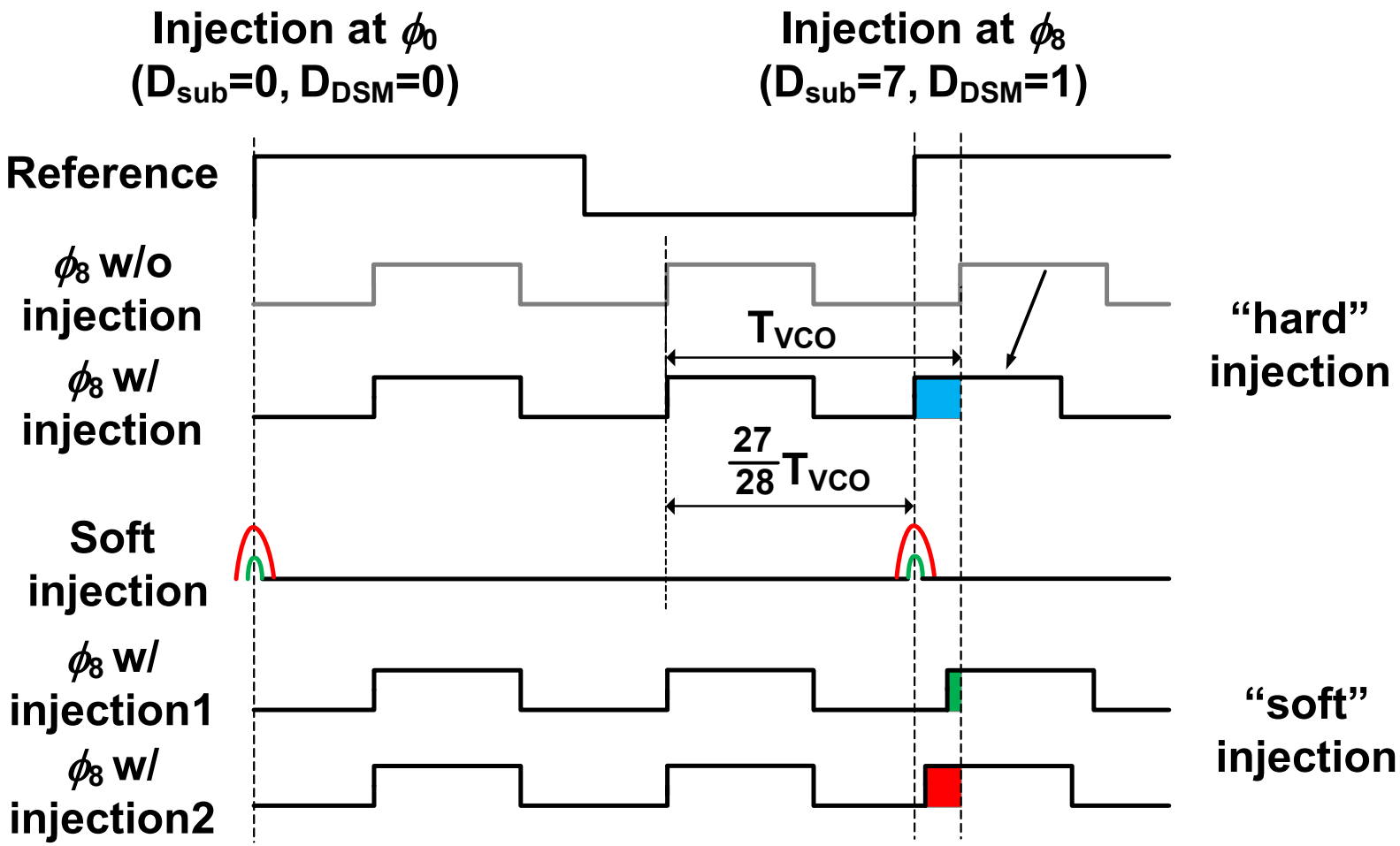


P0 → P0 → P1 → P1 → P2 → P2 → P3 …

Proposed Soft Injection

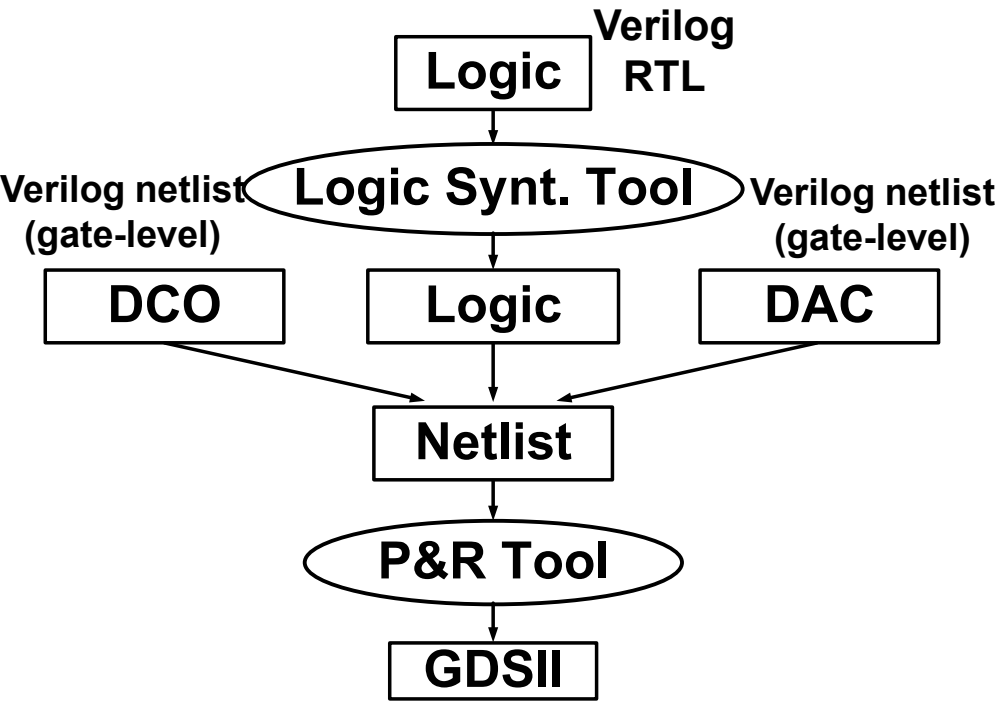


Proposed Soft Injection

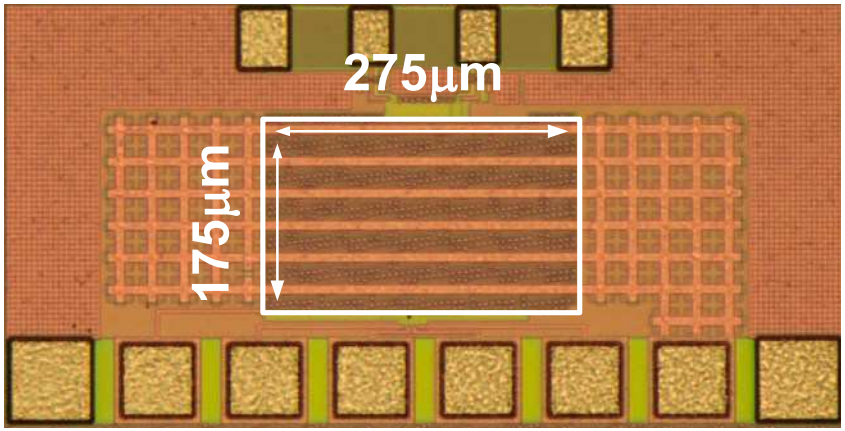


[W. Deng, *et al.*, ISSCC 2015]

Design Procedure and Chip Microphoto



Design Procedure



CMOS 65nm technology

Performance Comparison

	This work	Deng ISSCC2014	Marucci ISSCC2014	Elkholy ISSCC2014
CMOS Tech.	65nm	65nm	65nm	65nm
Power [mW]	3 @1.5222GHz	0.78 @0.9GHz	3 @1.7GHz	10.5 @0.58GHz
Spur [dBc]	-53	-47	-51	N/A
FoM [dB]	-224.2	-236.5	-232	-221.9
Type	Frac-*N*	Int-*N*	Frac-*N*	Frac-*N*
Topology	Soft Injection	Injection locking	DTC-based MDLL	Injection locking

*FOM is calculated based on RMS jitter. $\mathrm{FoM}=10\log[(\sigma_t/1\mathrm{s})^2(P_{DC}/1\mathrm{mW})]$

Conclusion

- A synthesizable fractional-*N* IL-PLL with a soft-injection locking technique is presented.

- The proposed fractional-N IL-PLL can achieve fine resolution, low spur with comparable FoM.