A 2.2GHz -242dB-FOM 4.2mW ADC-PLL using Digital Sub-Sampling Architecture

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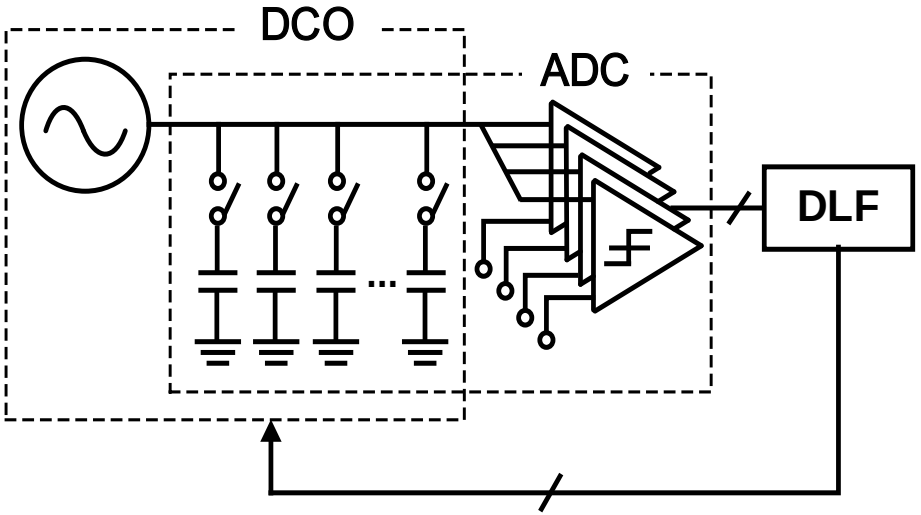
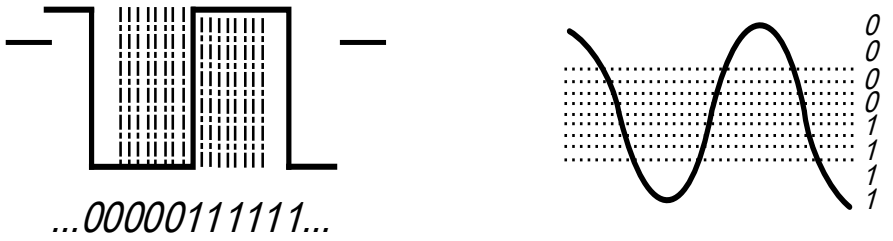
Conventional TDC based PLL⇒Power Jitter Trade-off

Proposed ADC based SS-PLL⇒Low Power and Low Jitter

Proposed Circuit





TDC-PLL(conventional)　　ADC-PLL(proposed)

Time Resolution vs. Power Consumption