Automated Design Strategy for High Performance Mixed Signal Circuits

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Matsuzawa & Okada Lab.

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- **Background and basic strategy for automated design of mixed signal IPs**
- **Scalable 12bit SAR ADC for versatile uses**
- **Layout-driven circuit design and automated layout with regularity**
- **Fully synthesizable PLL IPs like digital logic gates**
- **Summary**

Background and basic strategy for automated design of mixed signal IPs

Analog front-end and M/S circuits

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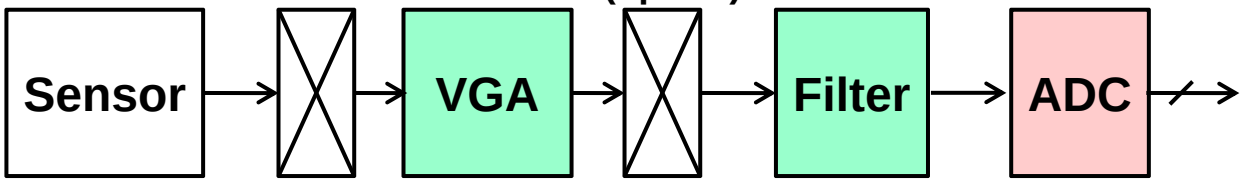
Analog front-end can be composed with a few types of mixed signal circuits; only ADC, DAC, PLL, Amplifiers (VGA, Filter) .

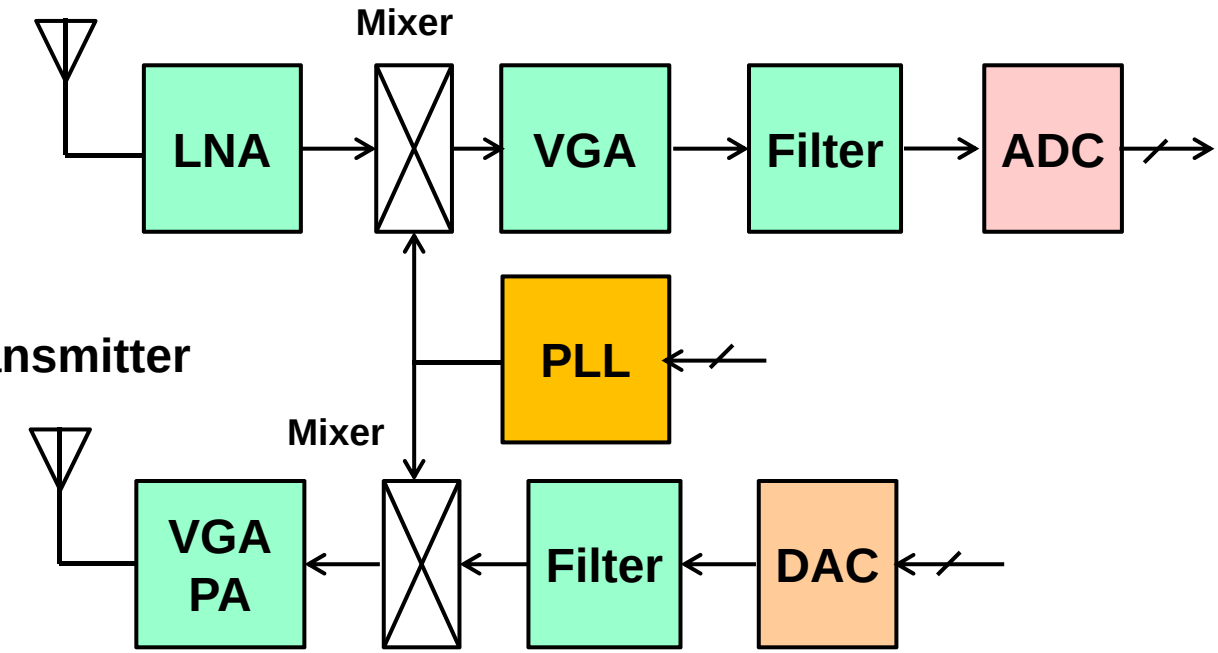
M/S: Mixed Signal

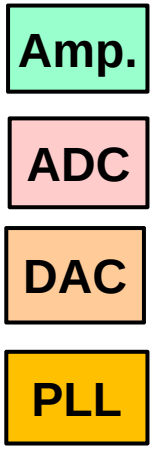
1) Sensor systems



2) Receiver

3) Transmitter





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Background and Motivation

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- **Issues**

  It becomes more difficult to obtain good M/S IPs

  - **Insufficient design resources (Designers, Tools)**
  - **Insufficient performance**
  - **Expensive**
  - **Longer development time**

M/S: Mixed Signal

- **Proposed solutions**
  - **Reduce # of M/S IPs → A few IPs for versatile uses**
  - **Scalable IPs: performance, power, design rule**
  - **Reduce the parasitic effect due to layout**
  - **Automated layout with regularity centric**
  - **Fully synthesizable IPs like digital logic gates**

Selection of the circuits

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Select the circuits for high performance automated design

- **Low voltage operation**
  - **Addressable with technology scaling**
- **Small occupied area**
  - **Reducible with technology scaling**
- **Low power**
  - **Scalable with performance**
- **Regularity in layout pattern**
- **Error can be compensated with digital method**

Scalable 12bit SAR ADC

for versatile uses

Scalable ADC

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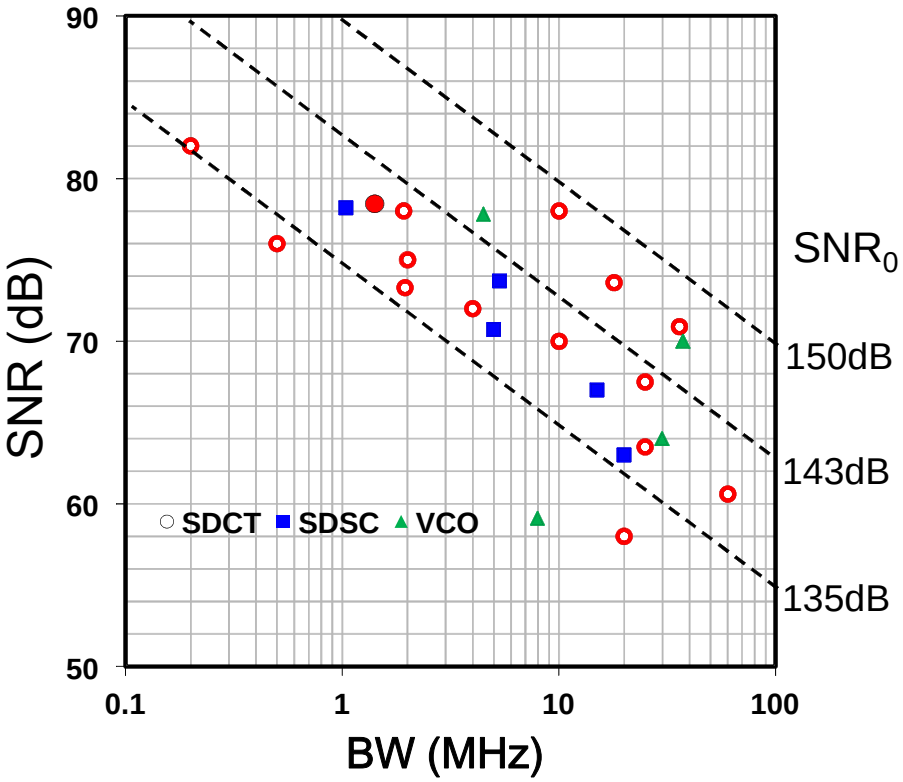
Many ADCs to cover the almost all wireless communications.

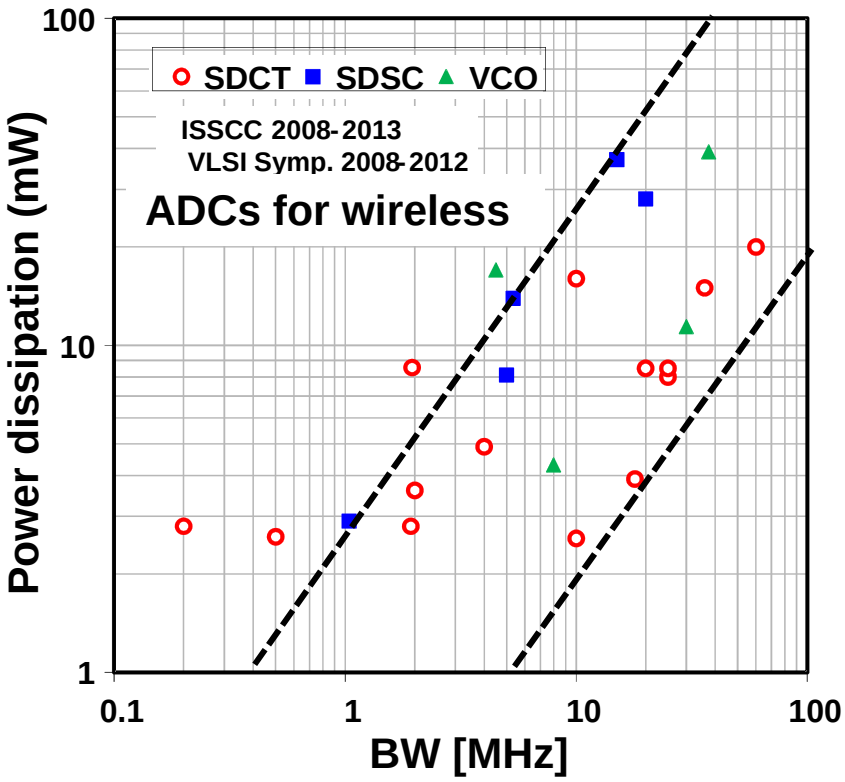
SNR should be increased by the reduction of BW
P_d should be minimized and reduced by the reduction of BW.

$$SNR \approx SNR_0 - 10\log(BW)$$

$$P_d \approx K_1 \cdot BW$$

K_1: 0.2 -- 3 (mW/MHz)





Matsuzawa, A. "Digitally-Assisted Analog and RF CMOS Circuit Design for Software-Defined Radio," Chapter 7, Springer 2011.

SAR ADC： ADC for versatile use

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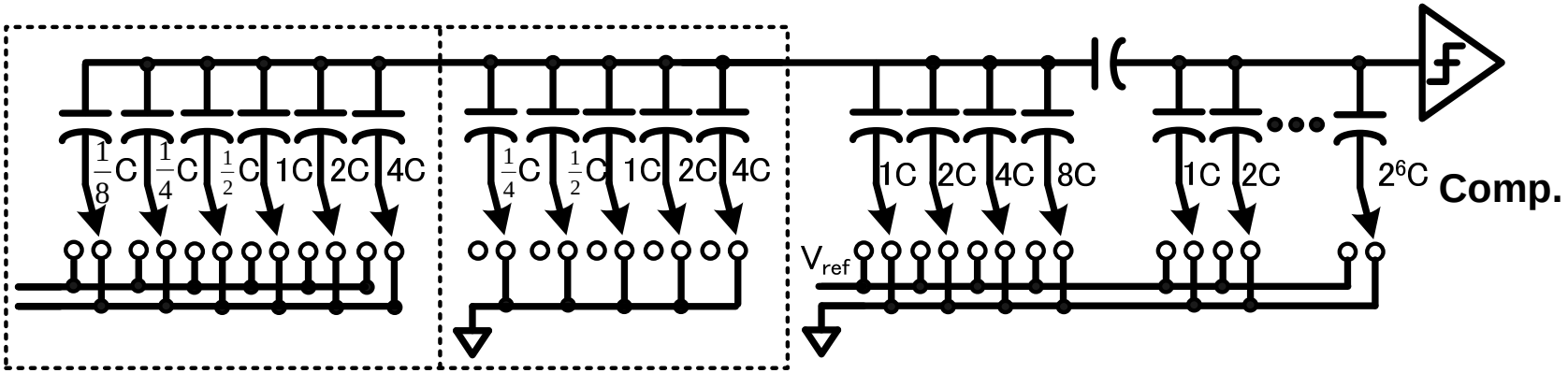
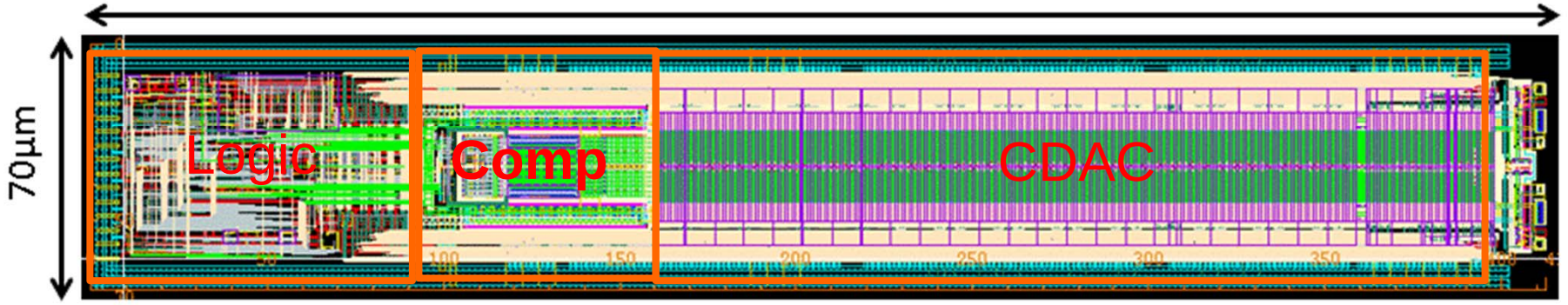
SAR ADC is the most energy efficient ADC.
It can be used for versatile applications.
Conversion errors can be suppressed digitally.



Mismatch CAL. **Parasitic CAL.** **12bit, 65nmCMOS, 0.03mm²**

S. Lee, A. Matsuzawa, SSDM 2013



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Use of MOM capacitor

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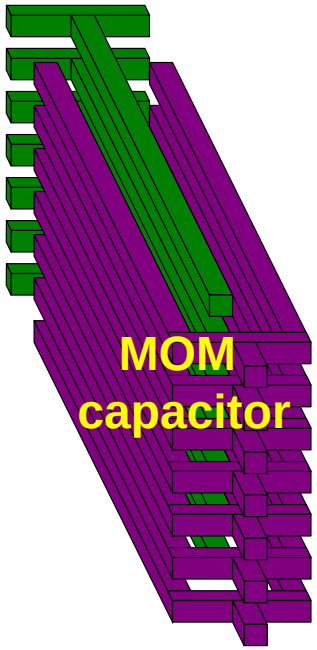
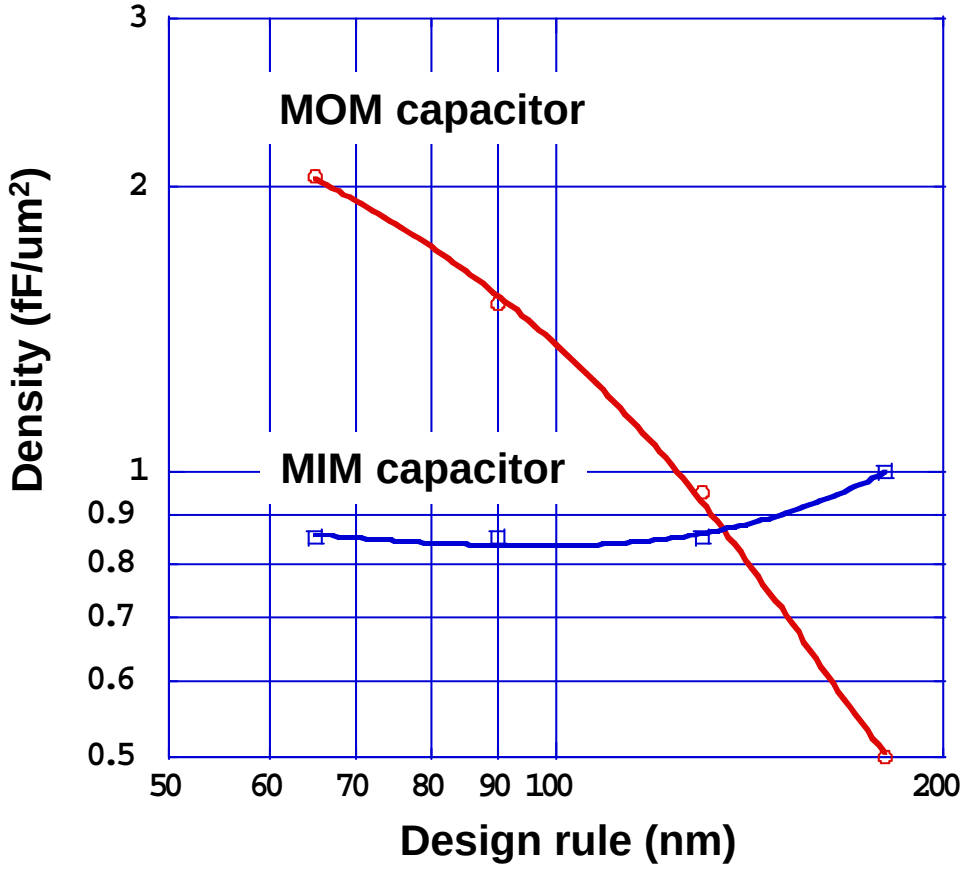
MOM capacitor uses the capacitance between the lateral interconnection.
The capacitor density can be increased by technology scaling.
Smaller occupied area (same C) can be expected by technology scaling.
Furthermore, parasitic capacitance can be controlled.





Dynamic comparator

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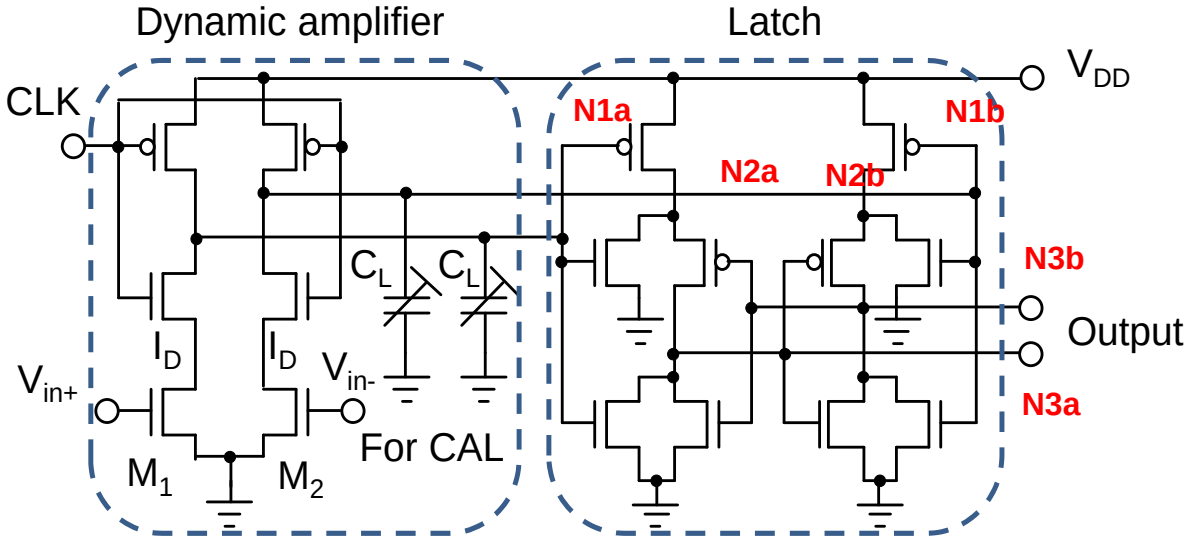
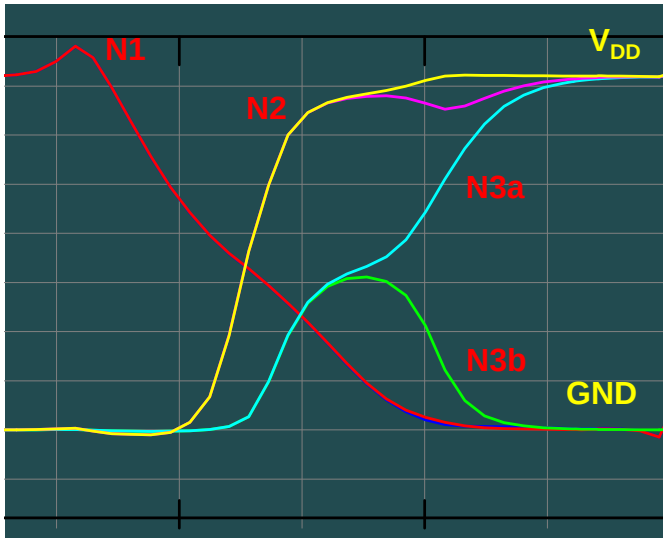
Dynamic comparator doesn't consume any static power.
Large noise was an issue, however can be improved by our proposed circuit using CMOS inter-stage amplifier.





M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, and Akira Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC," A-SSCC, 5-3, pp. 141-144, Taiwan, Taipei, Nov. 2009.

Intermitted operation by self-clocking

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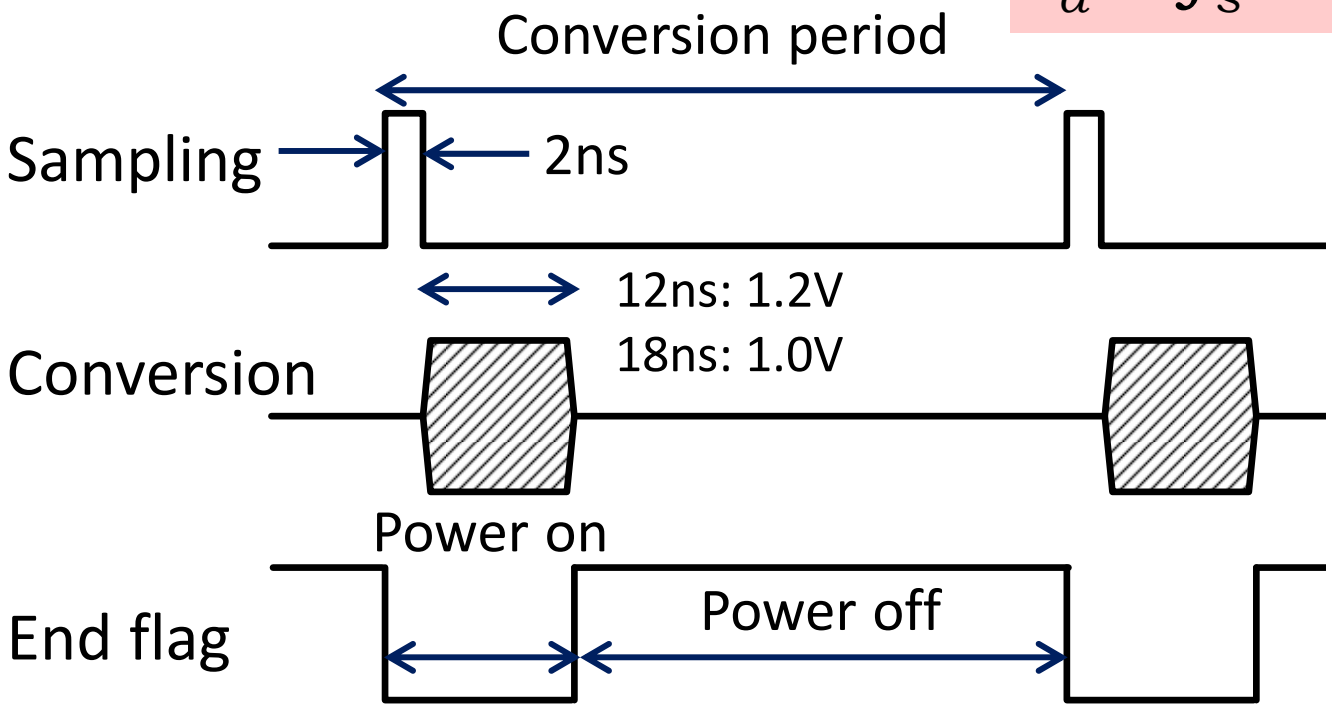
Successive comparison is started after the sampling period and ended at 12 conversions.
P_d is proportional to the sampling frequency.
The leakage current can be blocked by using power gating.

$$P_d = f_s \times E_d$$



Scalable power dissipation

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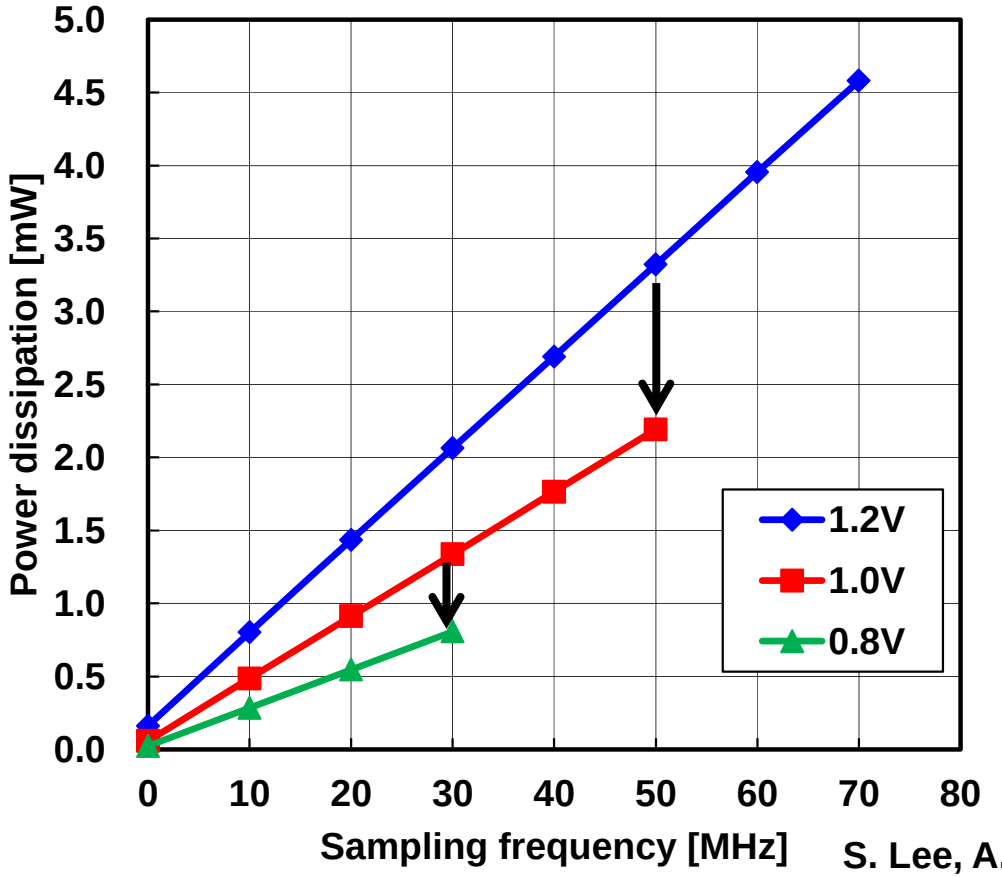
P_d is completely proportional to the sampling frequency.
Therefore an ultra-low power is possible at low speed operation.
Further low power is possible by using low voltage operation.

Suitable for the versatile uses; wireless and sensor



50MSps: 2mW
5MSps: 200uW
500KSps: 20uW
50KSps: 2uW
5kSps: 0.2uW

S. Lee, A. Matsuzawa, et al., SSDM 2013

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Performance comparison

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- **Highest conversion rate : 70MSps**
- **Lowest voltage : 0.8V**
- **Lowest P_d : 2.2mW at 50MSps**
- **Smallest FoM : 28fJ**
- **Smallest area : 0.03mm^2**

12bit SAR ADCs

	This work			[3]	[4]
Resolution (bit)	12			12	12
V_{DD} (V)	0.8	1	1.2	1.2	1.2
fsample (MHz)	30	50	70	45	50
Pd (mW)	0.8	2.2	4.6	3	4.2
SNDR (dB)	62	64	65	67	71
FoM (fJ) Nyq/DC	81/28	62/33	100/45	36/31	36/29
Technology (nm)	65			130	90
Occupied area(mm^2)	0.03			0.06	0.1

S. Lee, A. Matsuzawa, et al., SSDM 2013.
[3] W. Liu, P. Huang, Y. Chiu, ISSCC, pp. 380-381, Feb. 2010.
[4] T. Morie, et al., ISSCC, pp.272-273, Feb. 2013.

Performance scalable ADC

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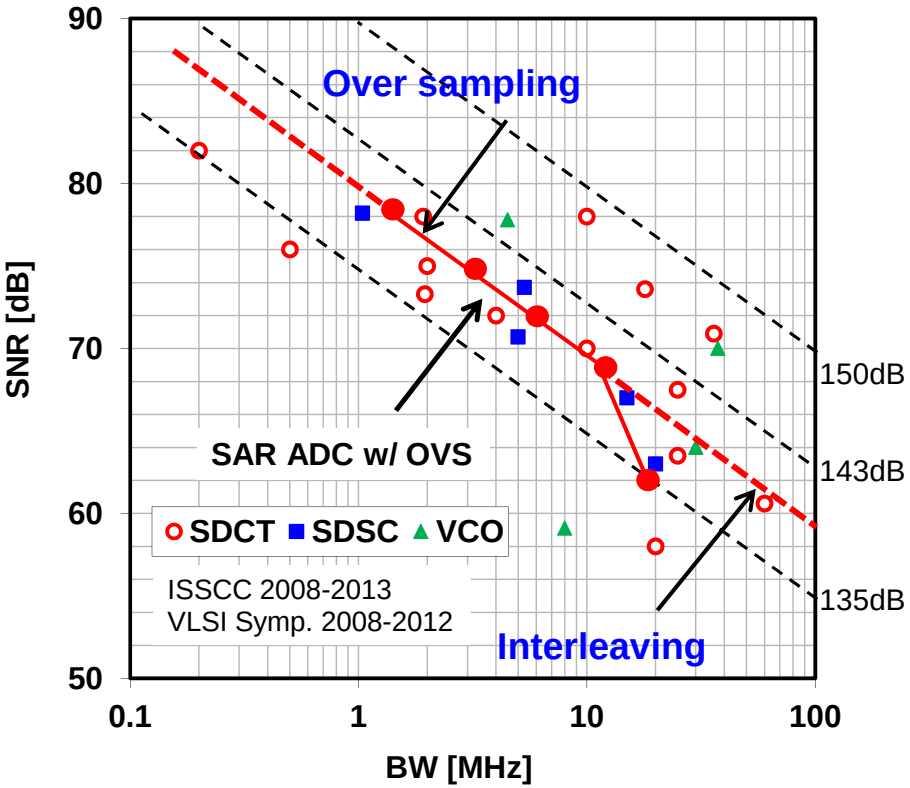
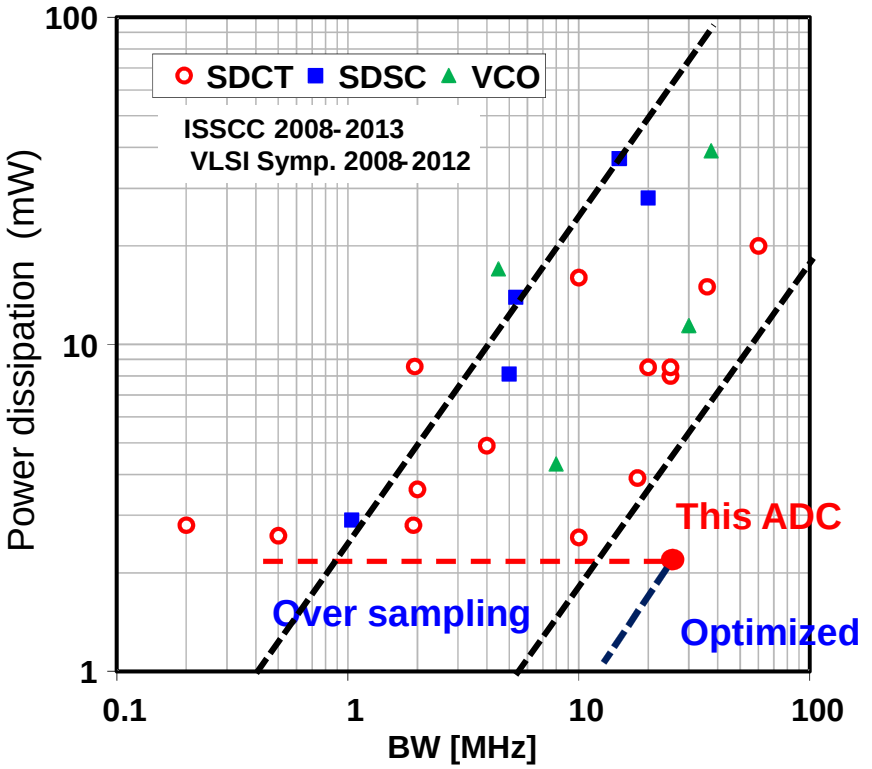
SNR can be increased up to 78 dB by reducing BW.
Smallest P_d among ADCs for wireless communications.

84 dB will be attained by dither and DEM method.
SNR_0 is 140 dB and it can be increased.

S. Lee, A. Matsuzawa, et al., SSDM 2013



1V, 50MSps Operation



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Layout-driven circuit design

and automated layout with regularity

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Conventional idea for analog IP design

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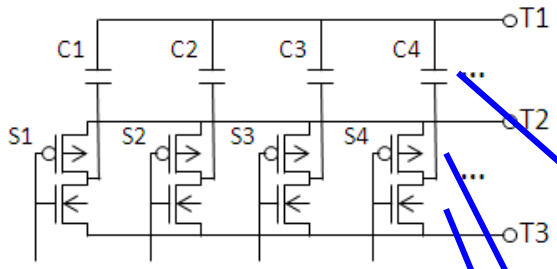
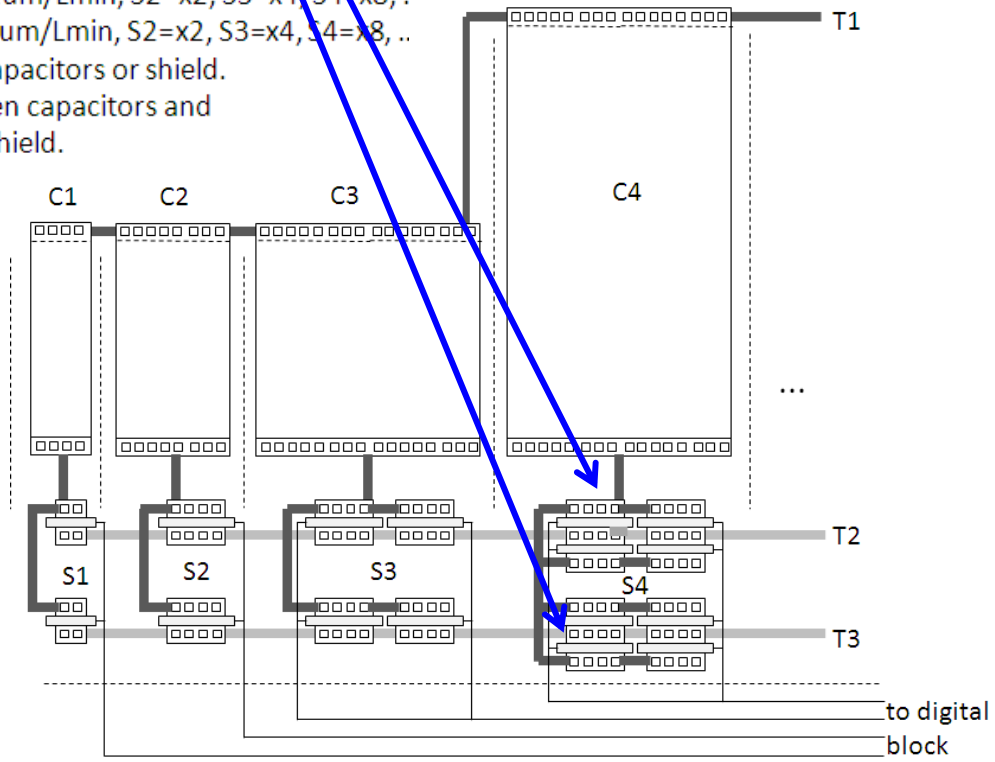


cell generator

Place the components
Route wires between them

1. C1=20fF, C2=40fF, C3=80fF, C4=160fF, ..
2. S1 NMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, .
3. S1 PMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, ..
4. Separate each capacitors or shield.
5. Separate between capacitors and digital block or shield.



Issue of conventional idea for analog design

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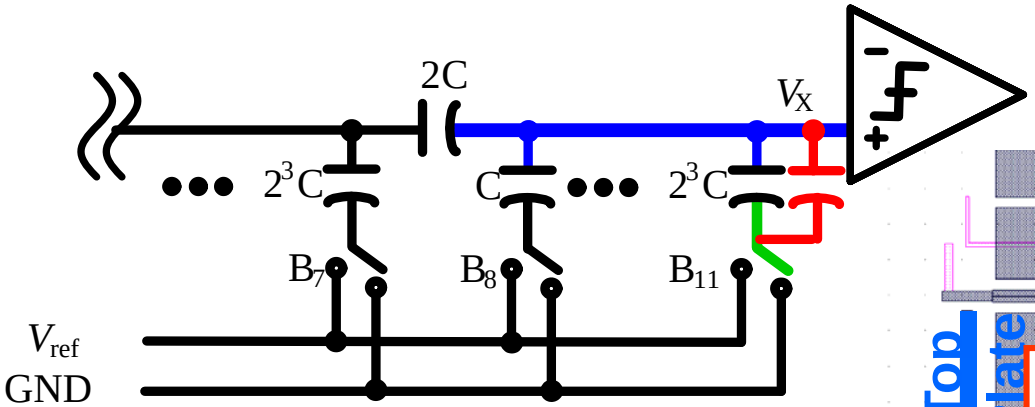
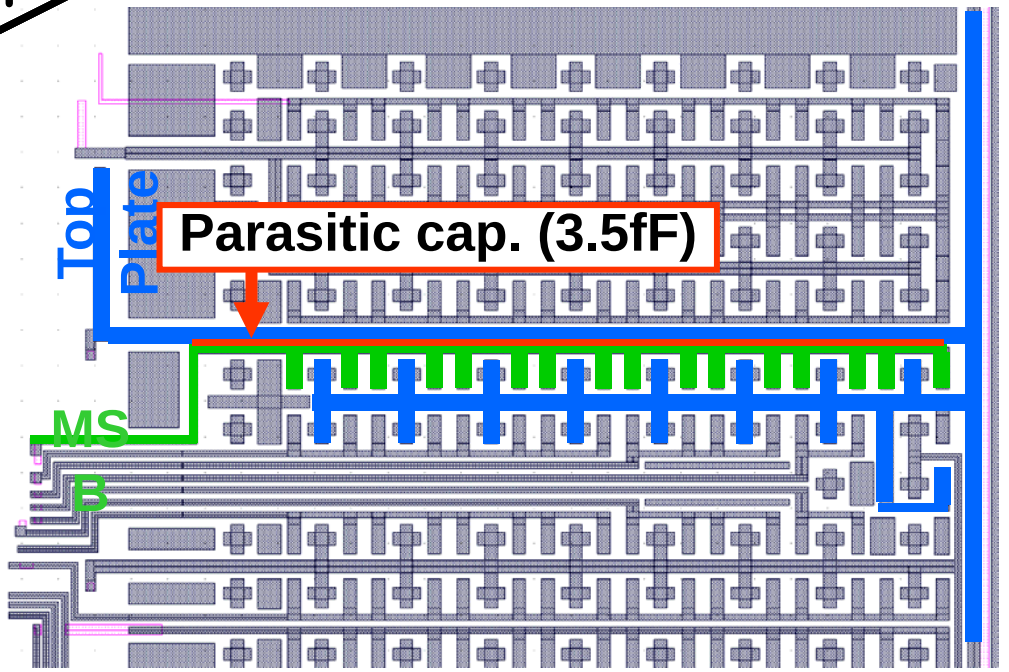
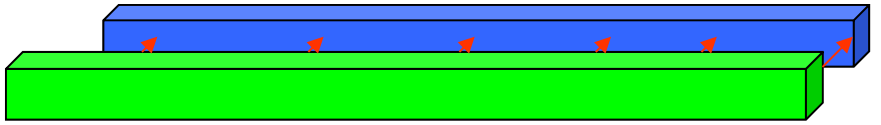
A conventional idea of Place the components and Route them causes parasitic components essentially and it results in performance degradation.



CDAC

Layout of CDAC





Parasitic capacitance (3.5 fF) Between top prate and bottom plates Causes large conversion error of 50 LSB (12 bit).

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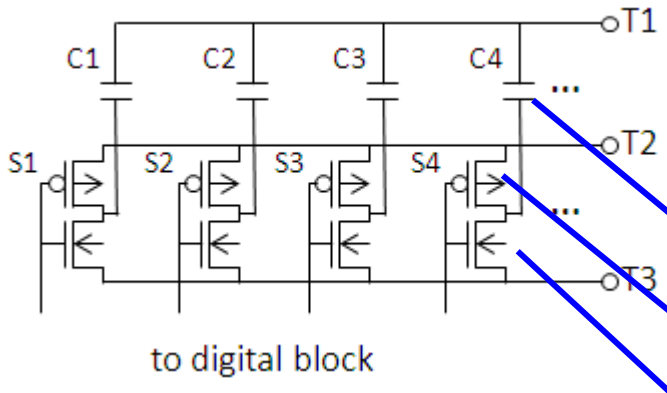
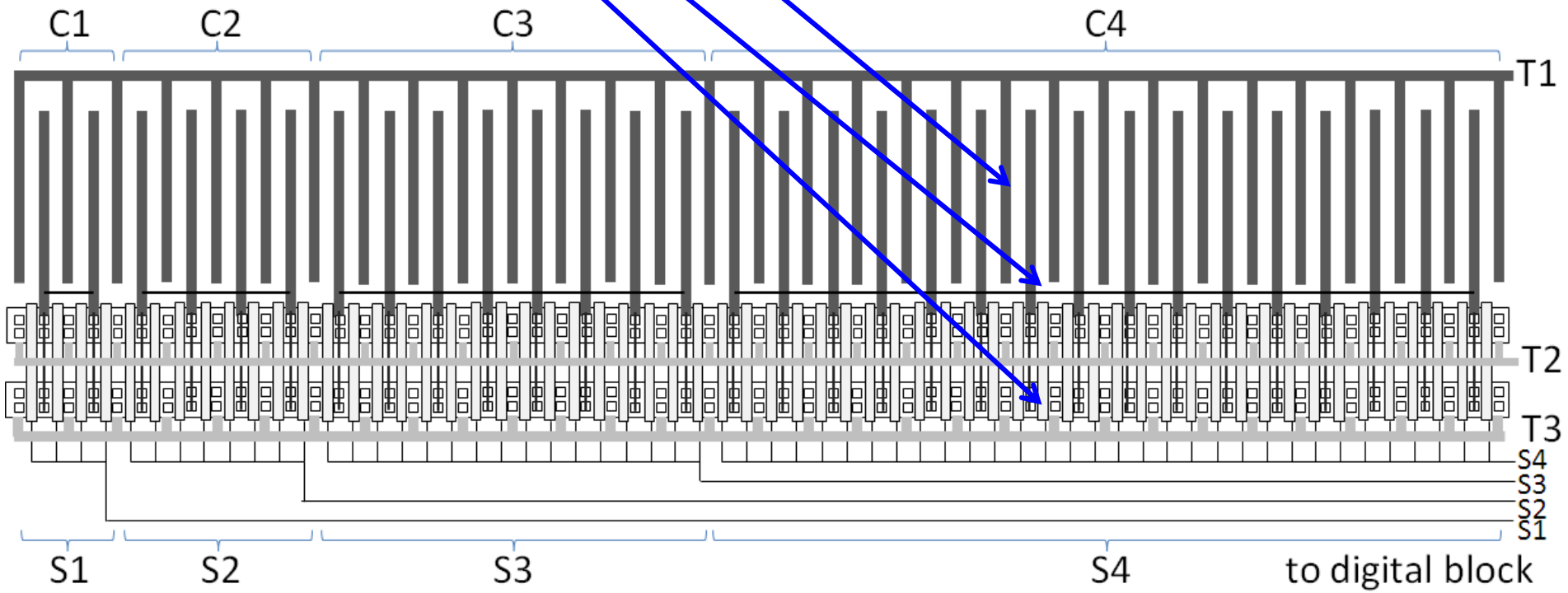
Layout driven design with regularity



Avoid wires between components
Wire itself is the component
Respect the regularity and
Pitch should be aligned

Furthermore, if layout has a regularity,
Layout programming becomes easier



Ideal layout design

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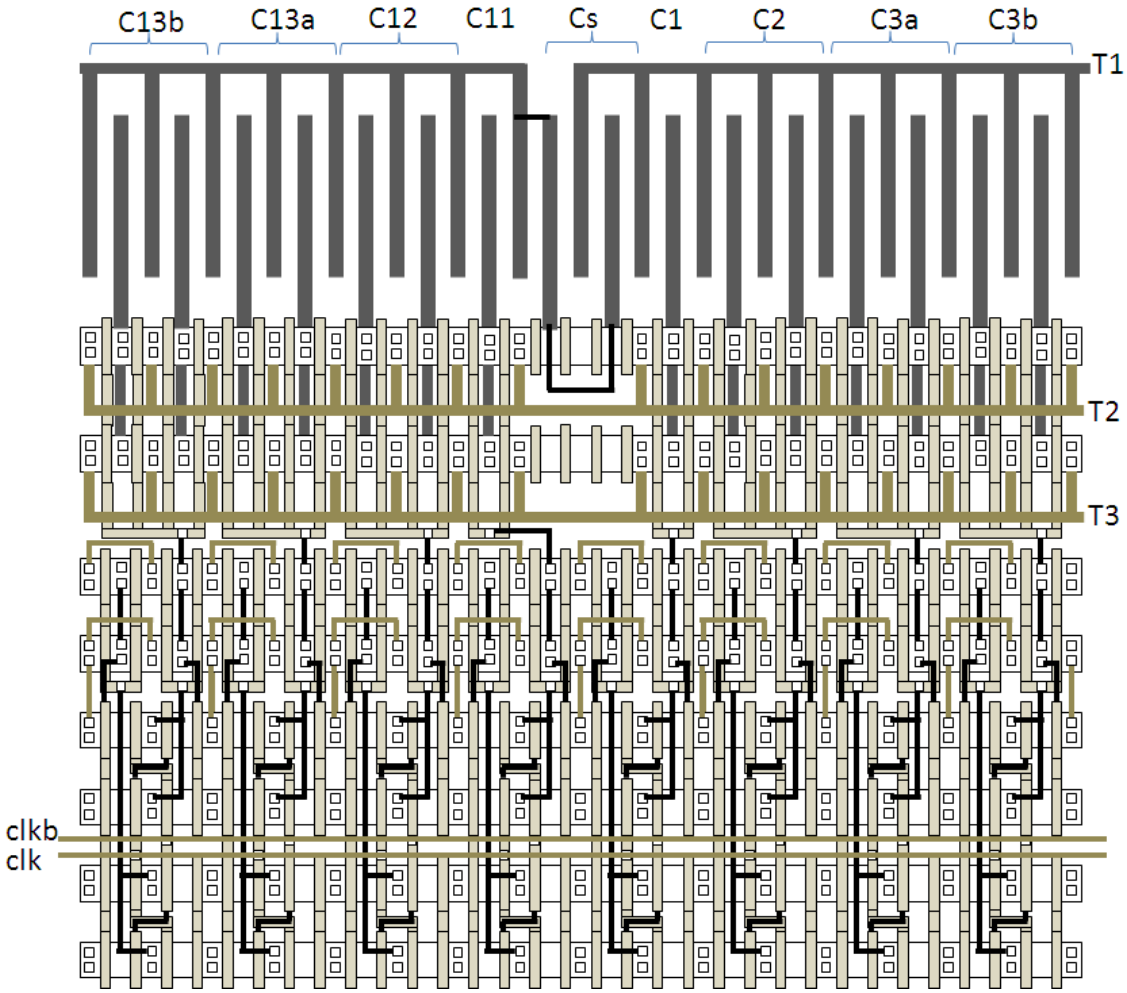
Pitch is aligned.
It minimizes parasitic component , wire length, delay and capacitance.
Low power, high speed, small area, and high robustness can be realized.



SAR ADC

Synthesized layout

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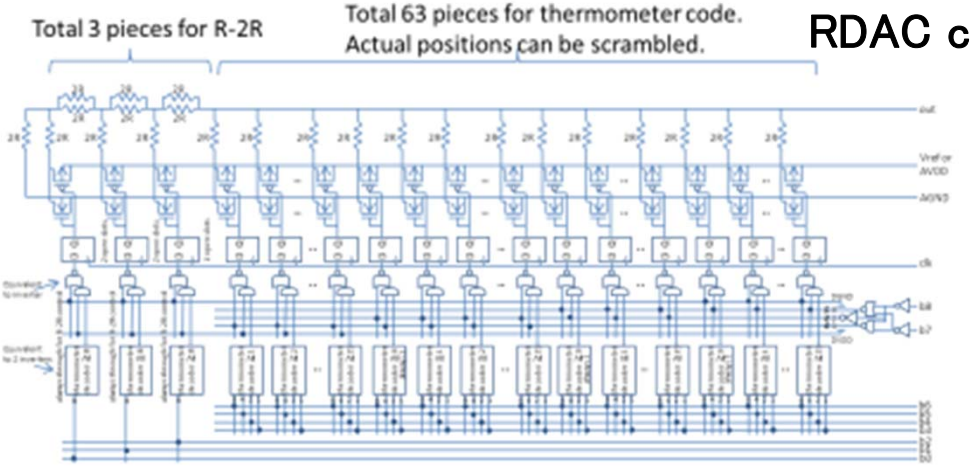
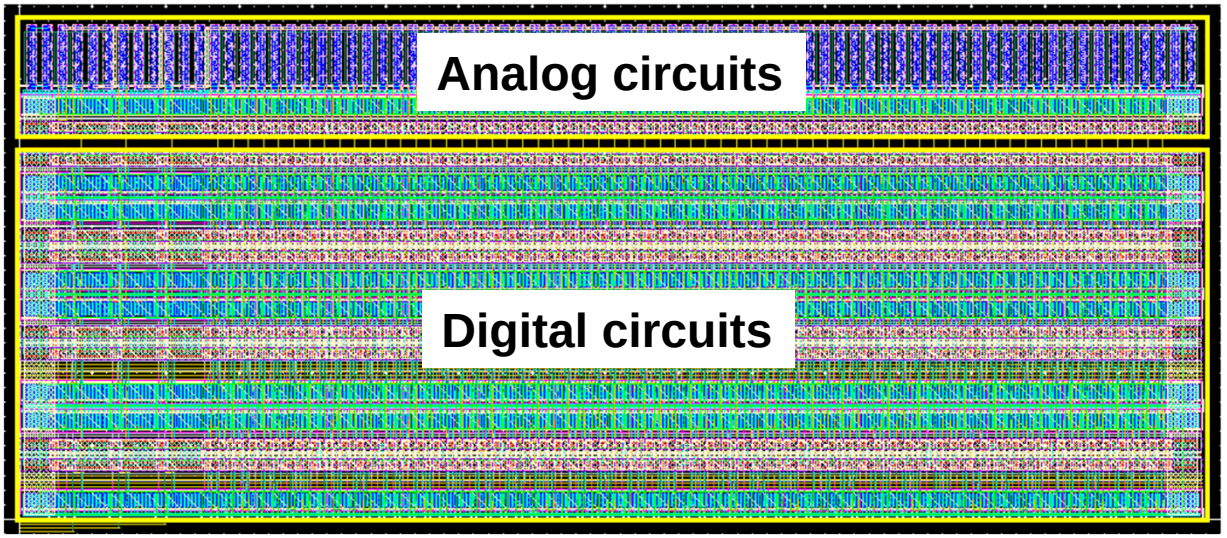
We can synthesize analog layout by programming



Automated optimization
Automated layout with SKILL language

RDAC layout composed by the programming in skill language



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Design flow for mixed signal IP synthesis

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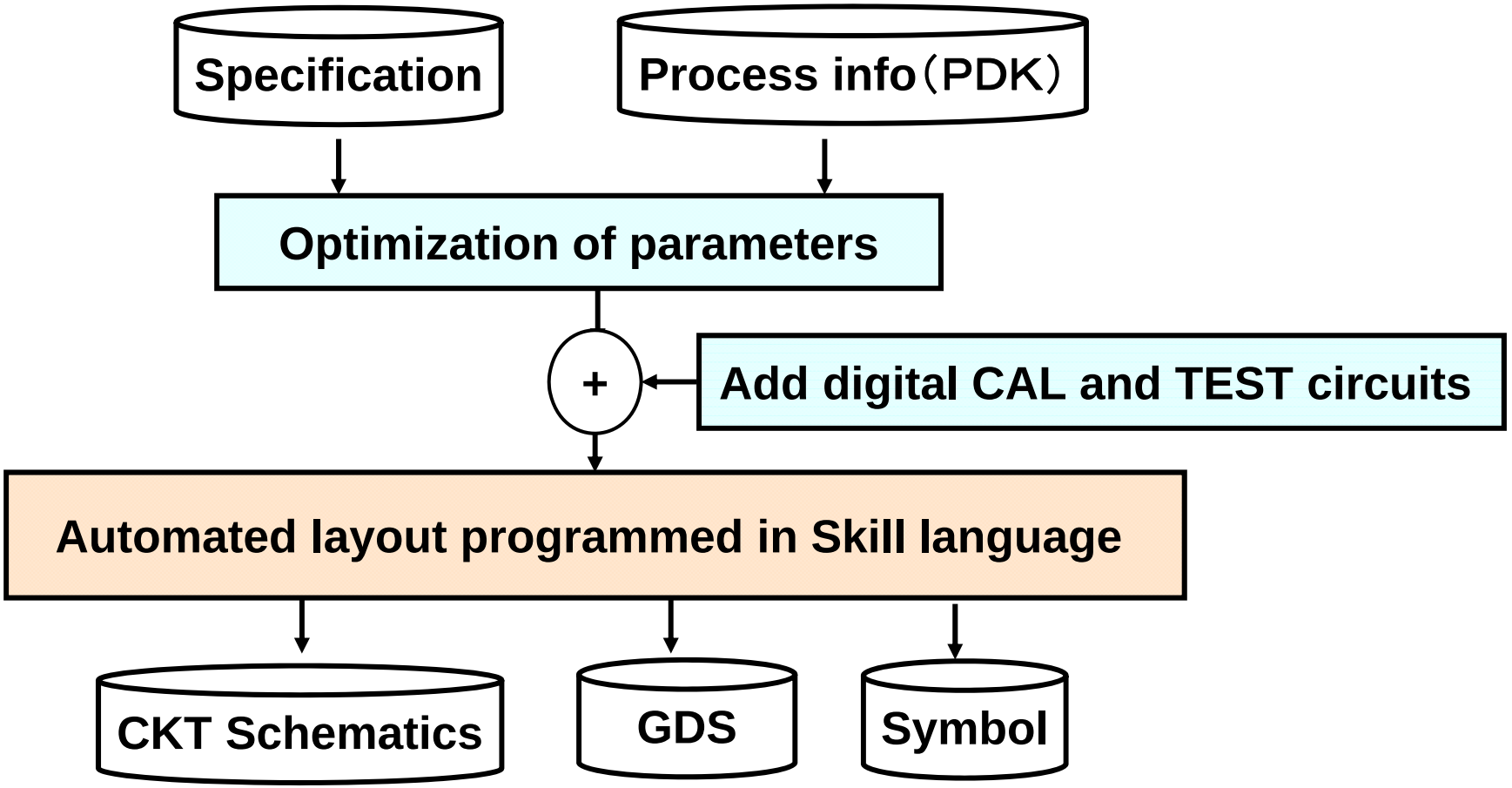
Automated design for circuit and layout



Circuit schematic and layout

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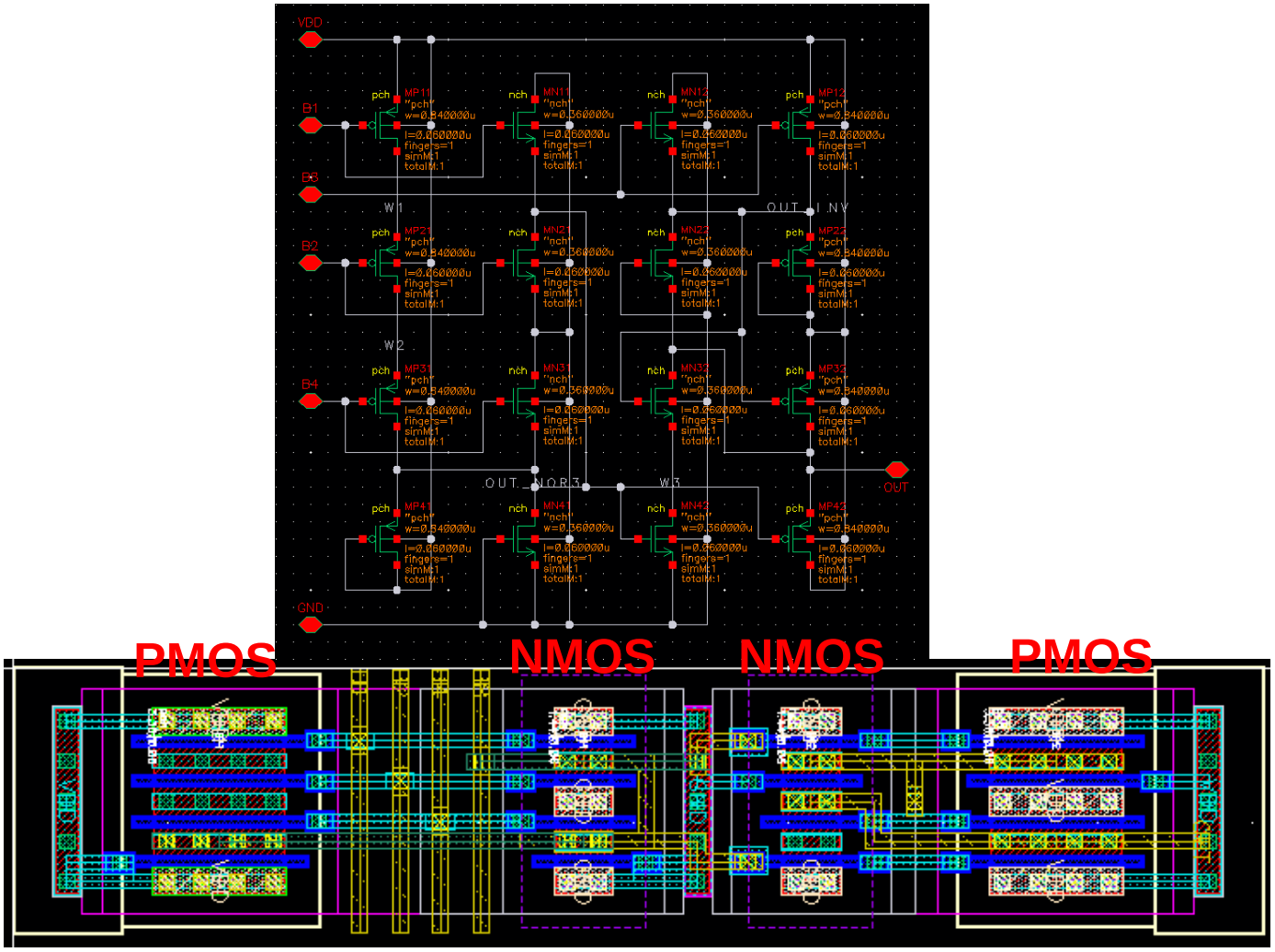
Logic gates should have regularity and launch the automated layout.



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Align the layout pitch

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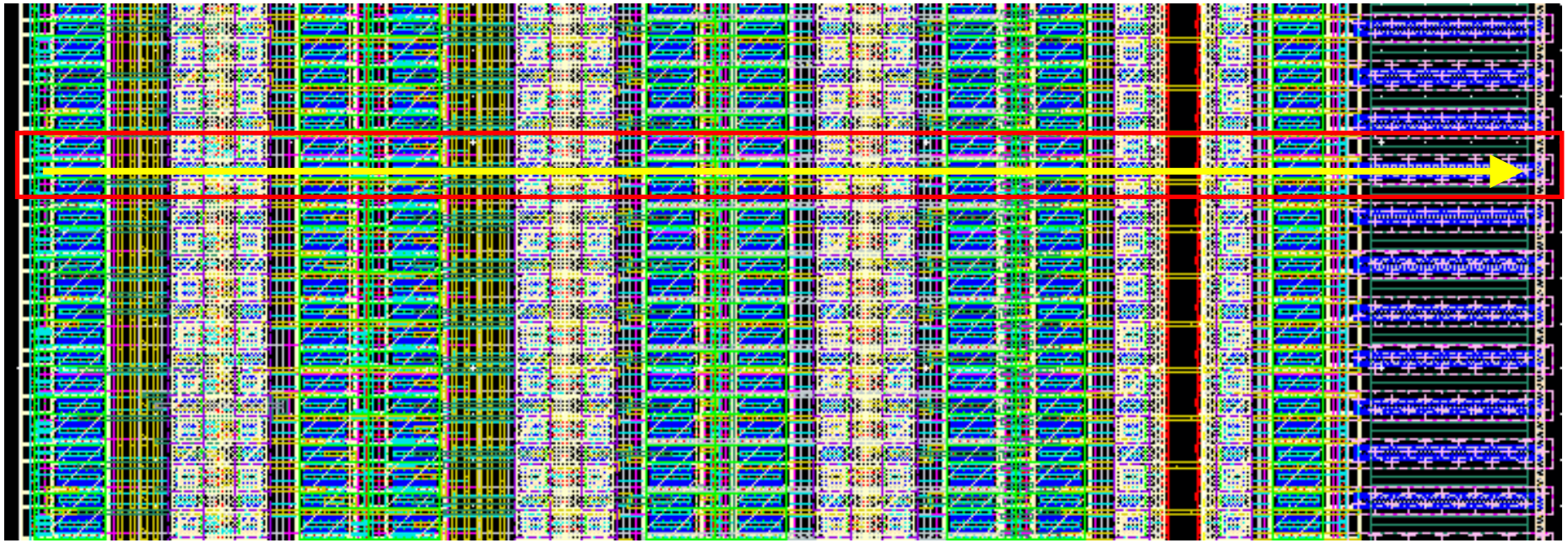
Logic gates, DFFs, switches, and resistors are aligned



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12 bit R-DAC with automated design

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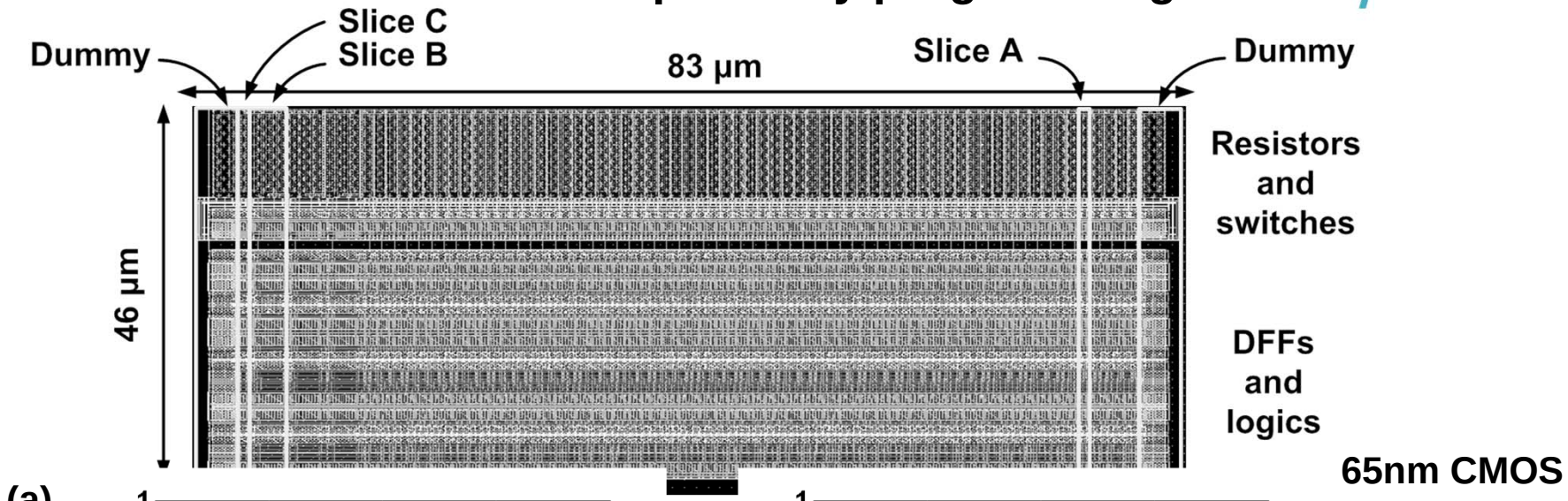
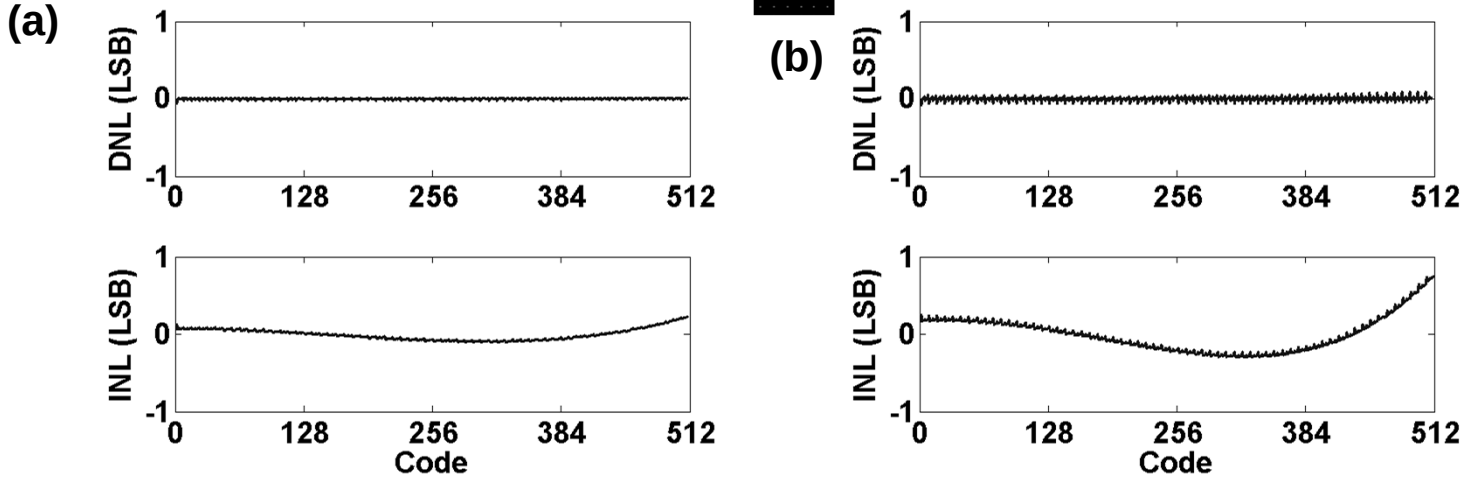
Small 12b R-DAC can be composed by programming in Skill





Simulated DNL and INL (a) without LPE, and (b) with LPE.

LC VCO with MOM capacitor bank

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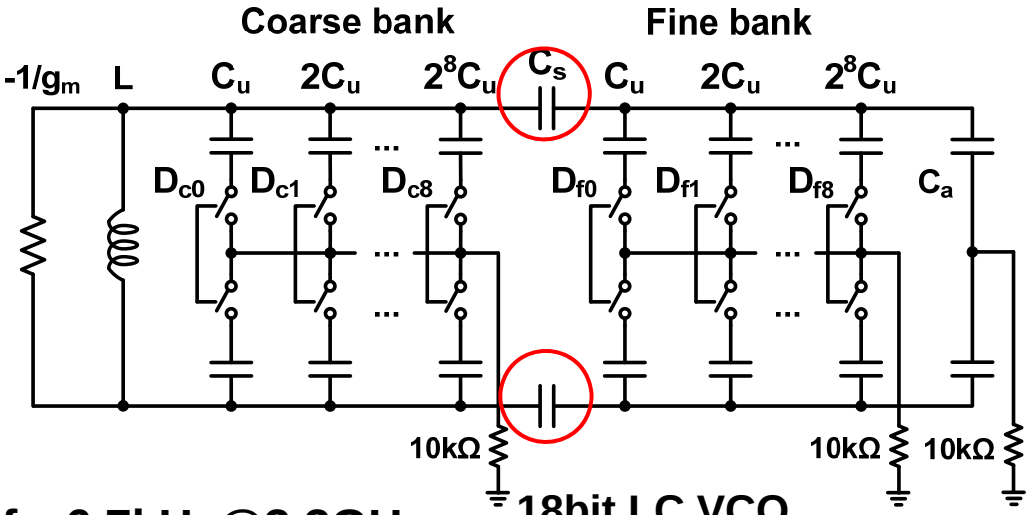
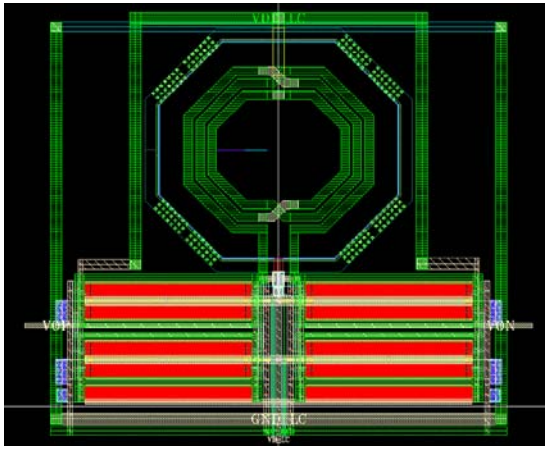
18bit LC VCO without varactors has been developed with MOM capacitors using by programed layout method

Z. Xu, A. Matsuzawa, SSDM 2014.

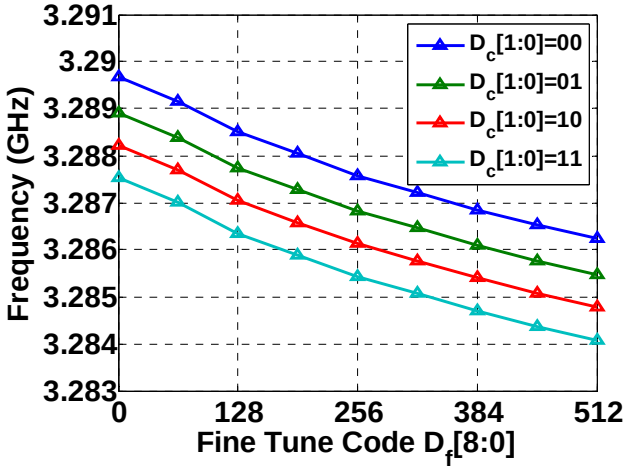


18bit LC VCO

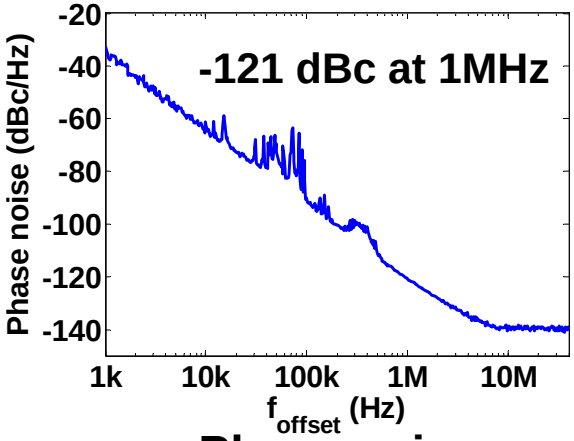


LC VCO 65nm CMOS

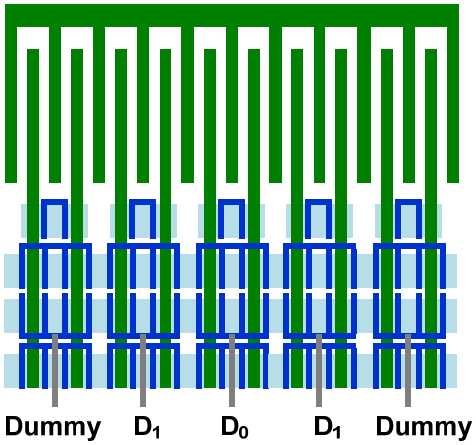
f_q=6.7kHz@3.3GHz



Fine tuning



Phase noise



MOM capacitance

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Fully synthesizable PLL IPs

like digital logic gates

Small, low jitter, and low power PLL for SoC

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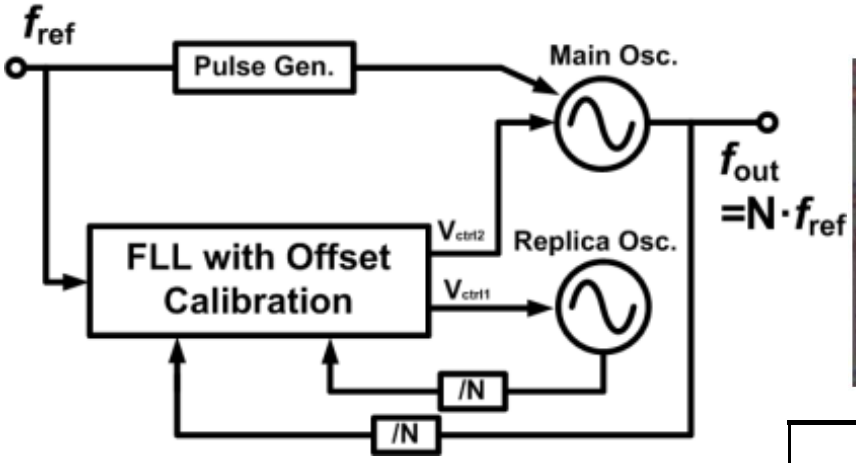
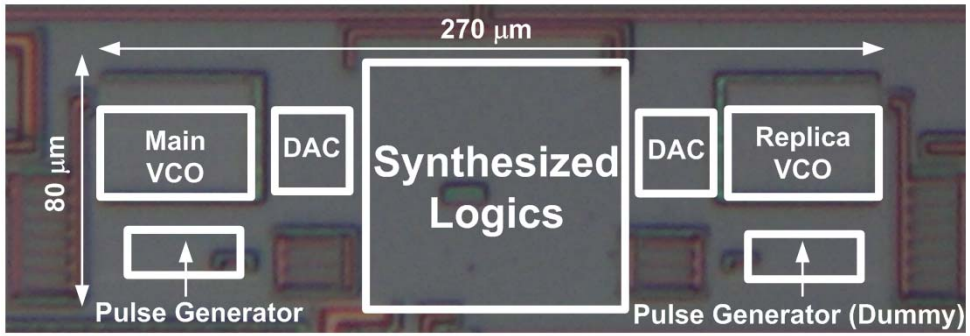
Small, low jitter, and low power PLL for SoC by using inject locking.

Tj=1.8ps, 1.0 mW, 0.02mm²



IL VCO Comparison

Automated circuit and layout design is possible.



	This work	[1]		[2]	[5]
	IL-PLL	DMDLL	DPLL	MDLL	IL-PLL
Freq. [GHz]	1.2 (0.5-1.6)	1.5 (0.8-1.8)	1.5 (0.8-1.8)	1.6	0.216
Ref. [MHz]	300 (40-300)	375	375	50	27
Power [mW]	0.97	0.89	1.35	12	6.9
Area [mm²]	0.022	0.25	0.25	0.058	0.03
Integ. Jitter [ps]	0.7	0.4	3.2	0.68	2.4
Jitter RMS/PP [ps]	1.81/19.4 10M hits	0.92/9.2 5M hits	4.2/33 5M hits	0.93/11.1 30M hits	N.A.
FOM [dB]	-243	-248.46	-228.59	-233.76	-225
CMOS Tech.	65nm	130nm	130nm	130nm	55nm

W. Deng, K. Okada, A. Matsuzawa, ISSCC 2013

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Injection-locked Ring Oscillator

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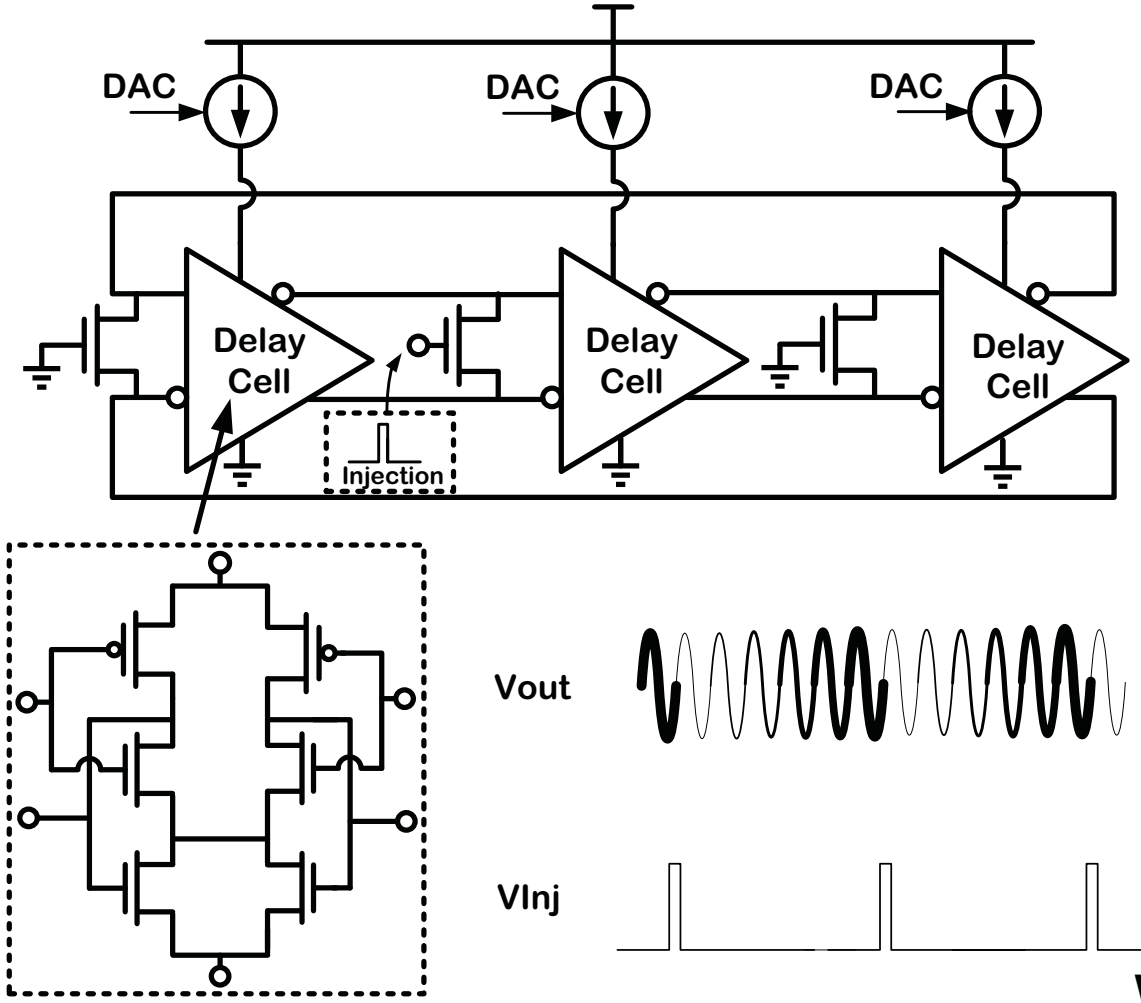
Differential ring VCO with injection locking



W. Deng. ISSCC 2013

Effect of the injection locking

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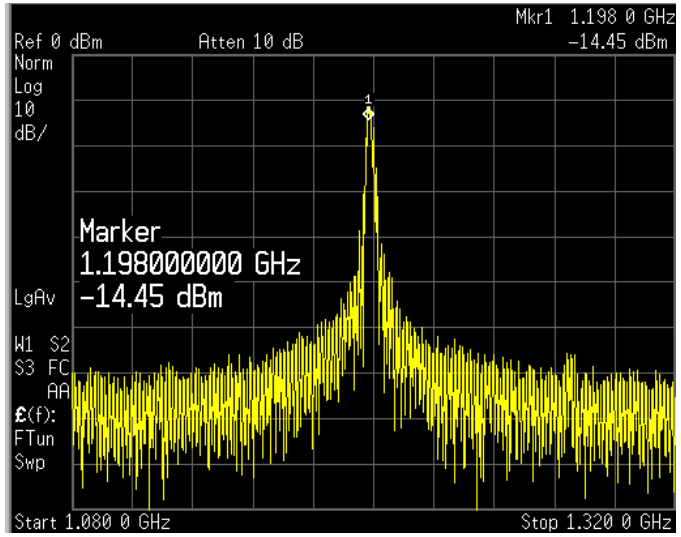
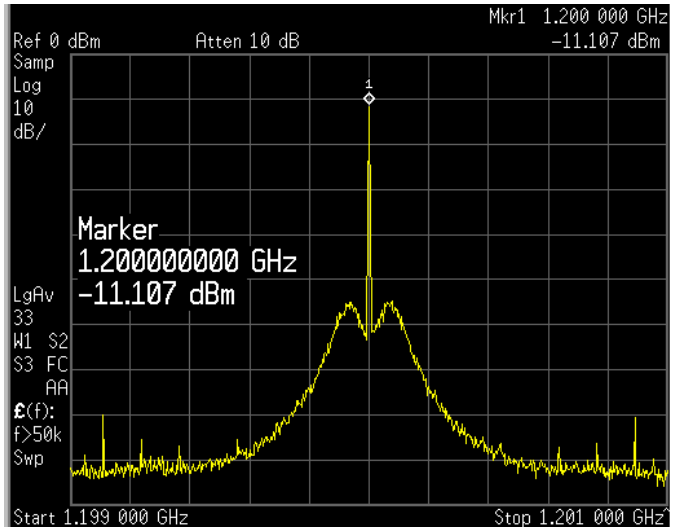
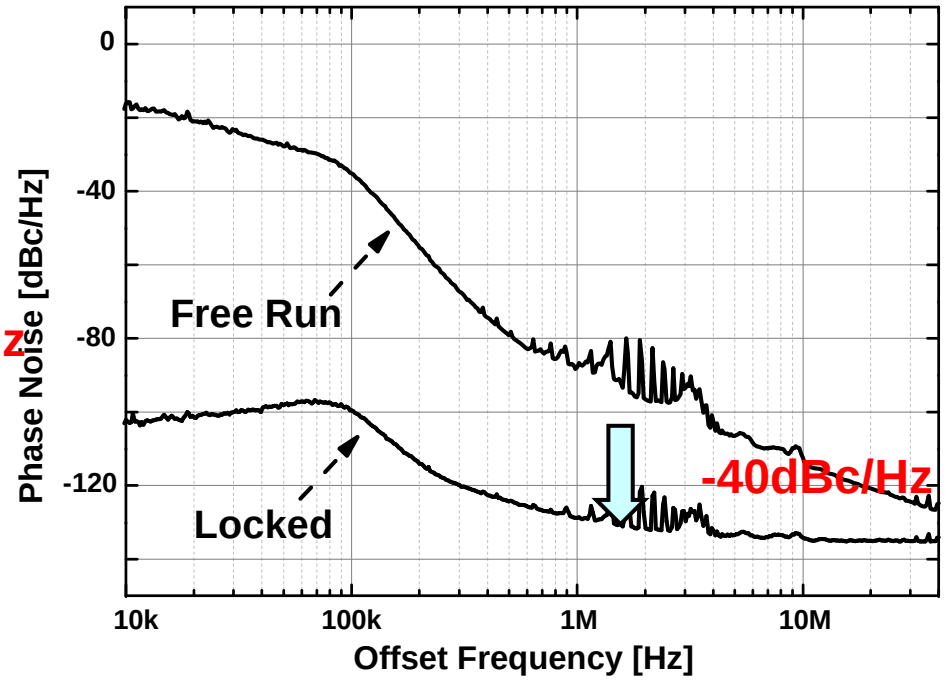


1.08GHz 1.32GHz



1.199GHz 1.201GHz

Phase noise is reduced so much by the injection locking



Ref.: 300MHz (40MHz-300MHz) Freq.: 1.2GHz (0.5-1.6GHz)
Integrated jitter: 0.7ps (10kHz-40MHz) Pdc: 0.97mW (1.2GHz)

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Automated design

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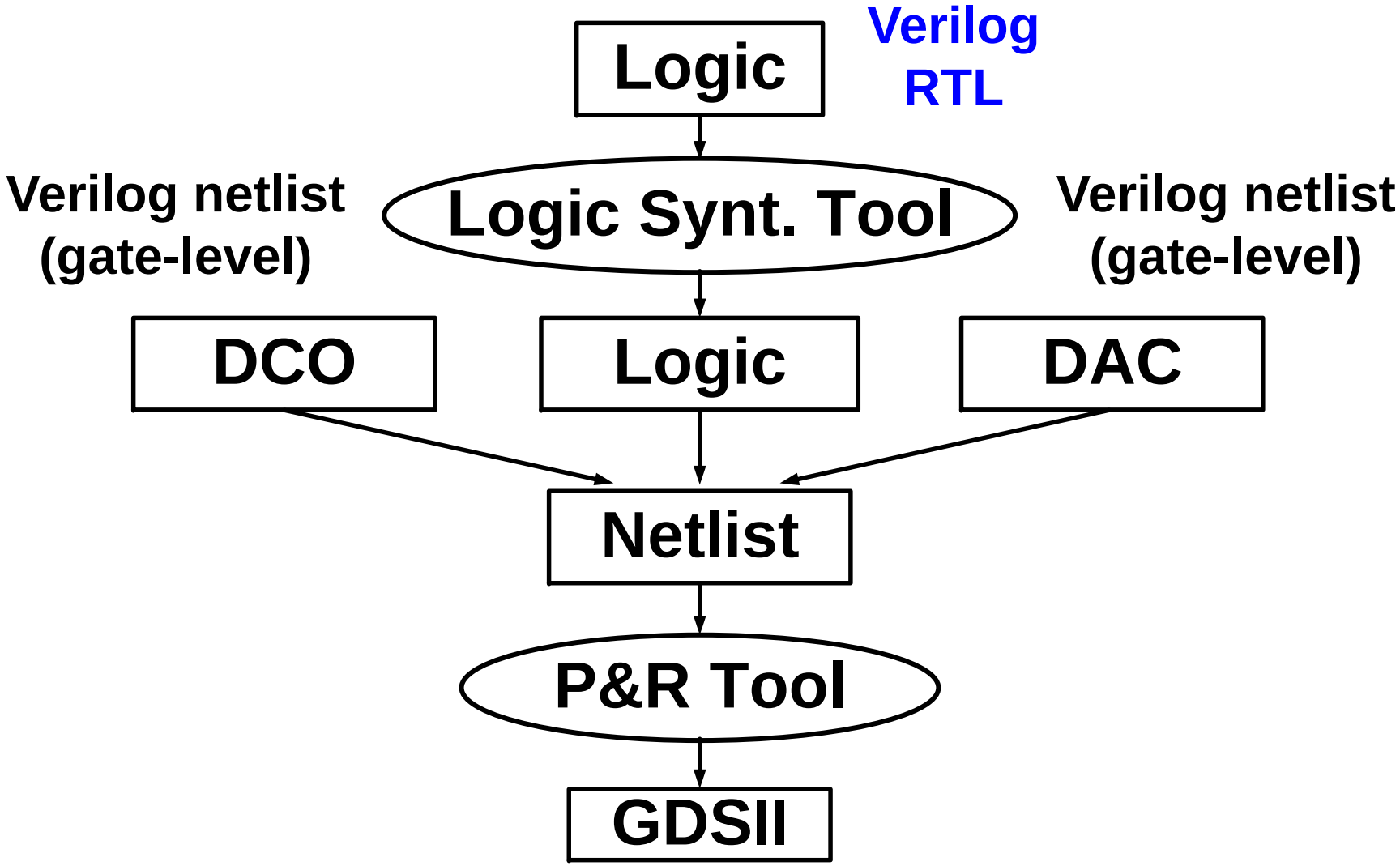
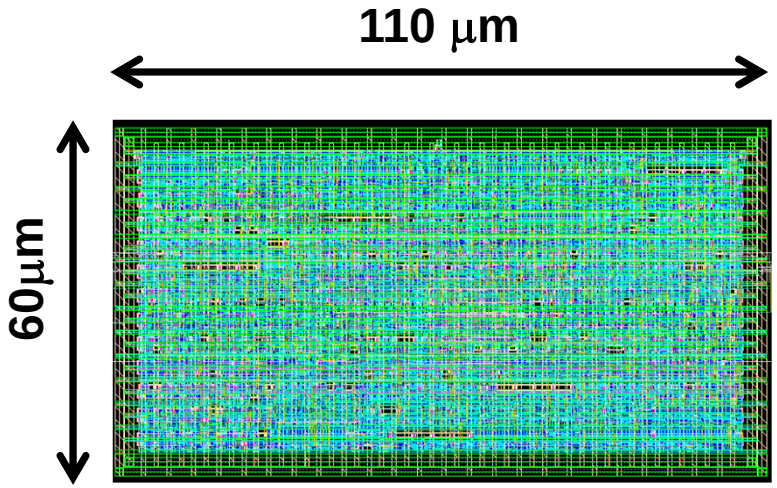
Automated design is possible like digital circuits with HDL.



Results

Low jitter, low power, and small area PLL can be realized with full automated design

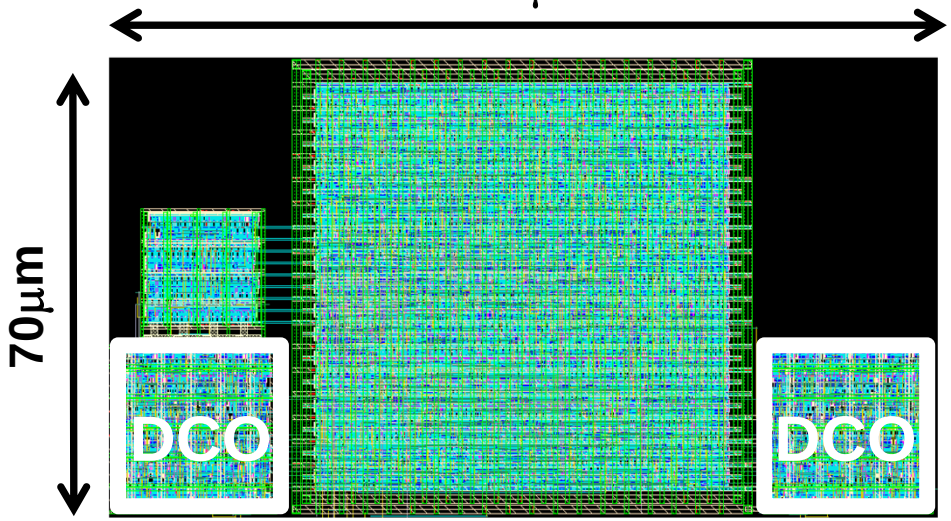
Integrating Jitter: 1.7ps
P_{DC}: 780μW
FOM: -236.5 dB



Fully synthesized

W. Deng, K. Okada, A. Matsuzawa, ISSCC 2014.

Integrating Jitter: 2.32ps
P_{DC}: 640μW
FOM: -234.6 dB



Hierarchical P&R with synthesized DCOs

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Performance Comparison

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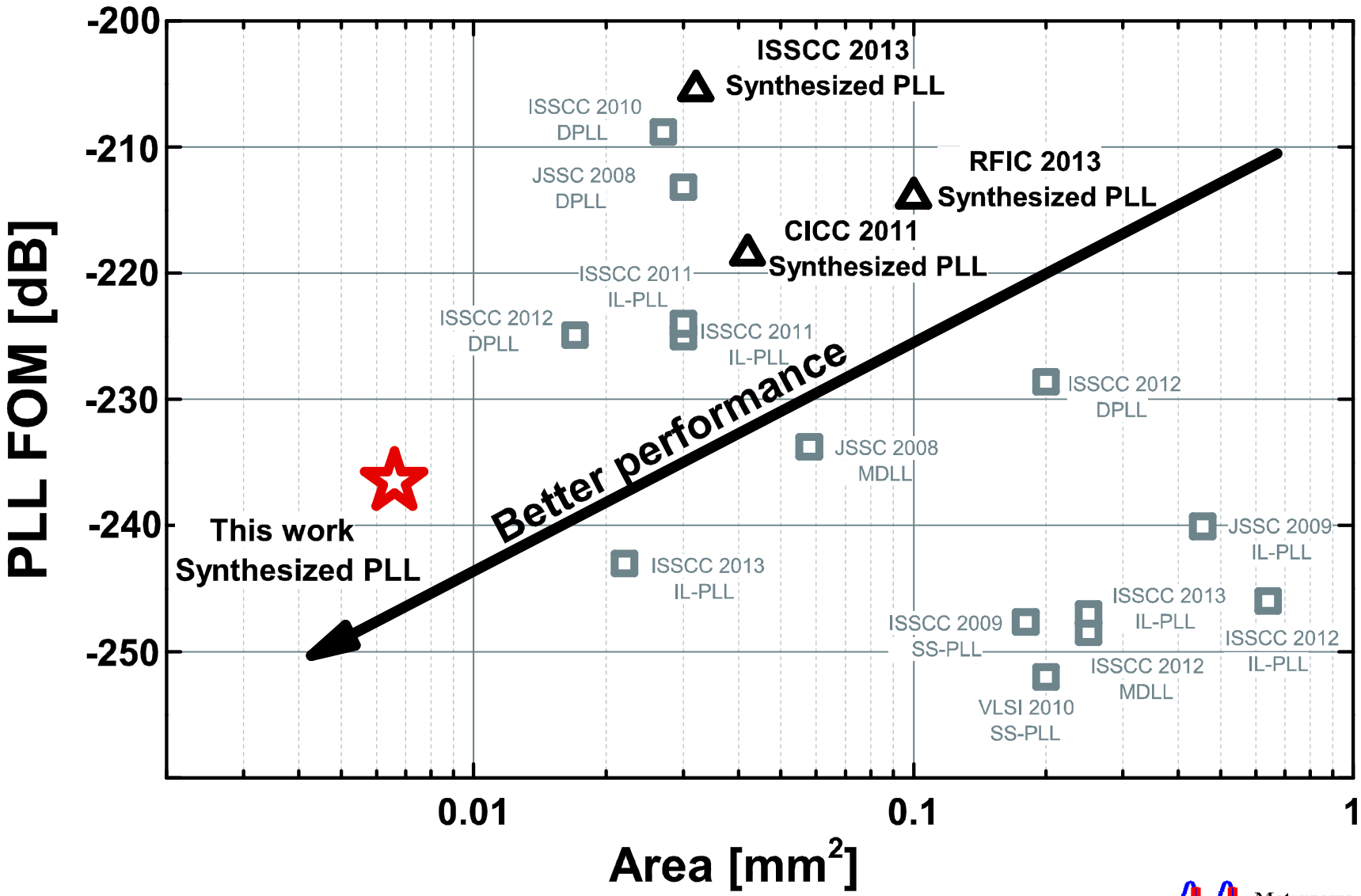
Low FoM and Small area Synthesizable PLL has been developed.



Proposed M/S IP design and business

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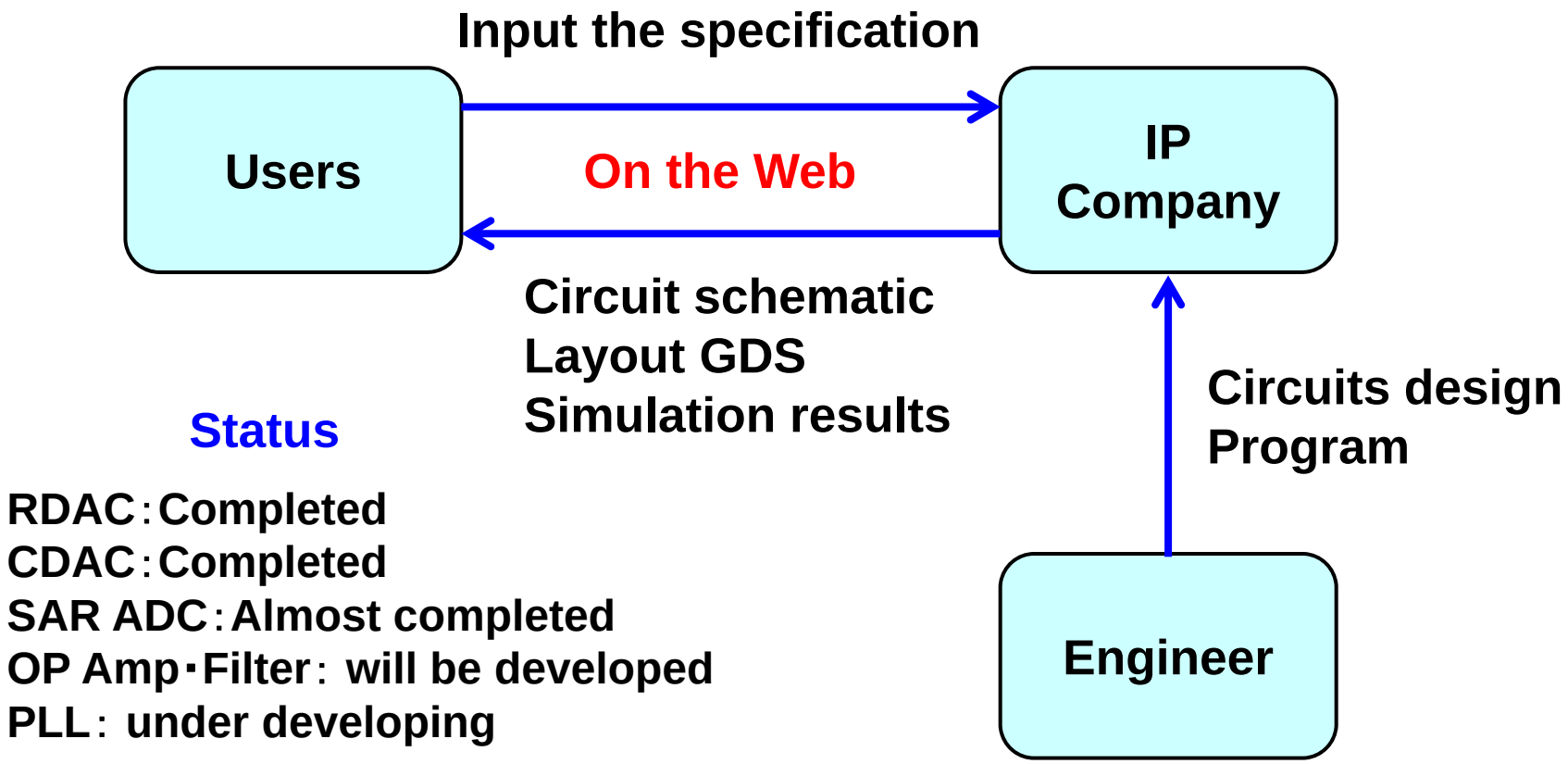
Circuits should be synthesized automatically.
Users can obtain M/S IPs immediately with less money.
No limitation for # of design requests



Status

RDAC：Completed
CDAC：Completed
SAR ADC：Almost completed
OP Amp・Filter： will be developed
PLL： under developing

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Summary

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- **Issues**

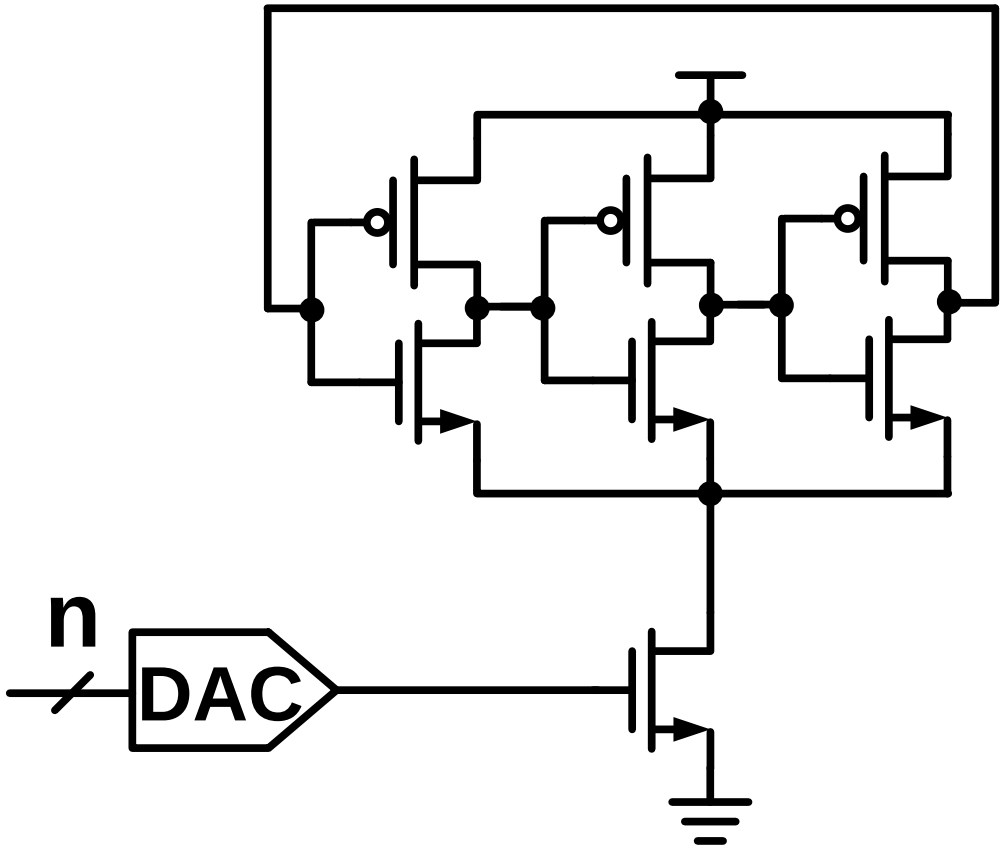
  It becomes more difficult to obtain good mixed signal IPs

- **Proposed solutions**
  - **A few mixed signal IPs for versatile uses**
    Ex: Scalable 12b SAR ADC for versatile use
  - **Regularity driven analog layout**
    - **Avoid wires between components by using wires as a component**
    - **Respect the regularity and pitch should be aligned**
  - **Developed the synthesizable mixed signal IPs programmed in Skill language**
  - **Developed synthesizable full automated PLL using injection locking, like digital logic design**
  - **It may create a new IP business model?**

Backup slides

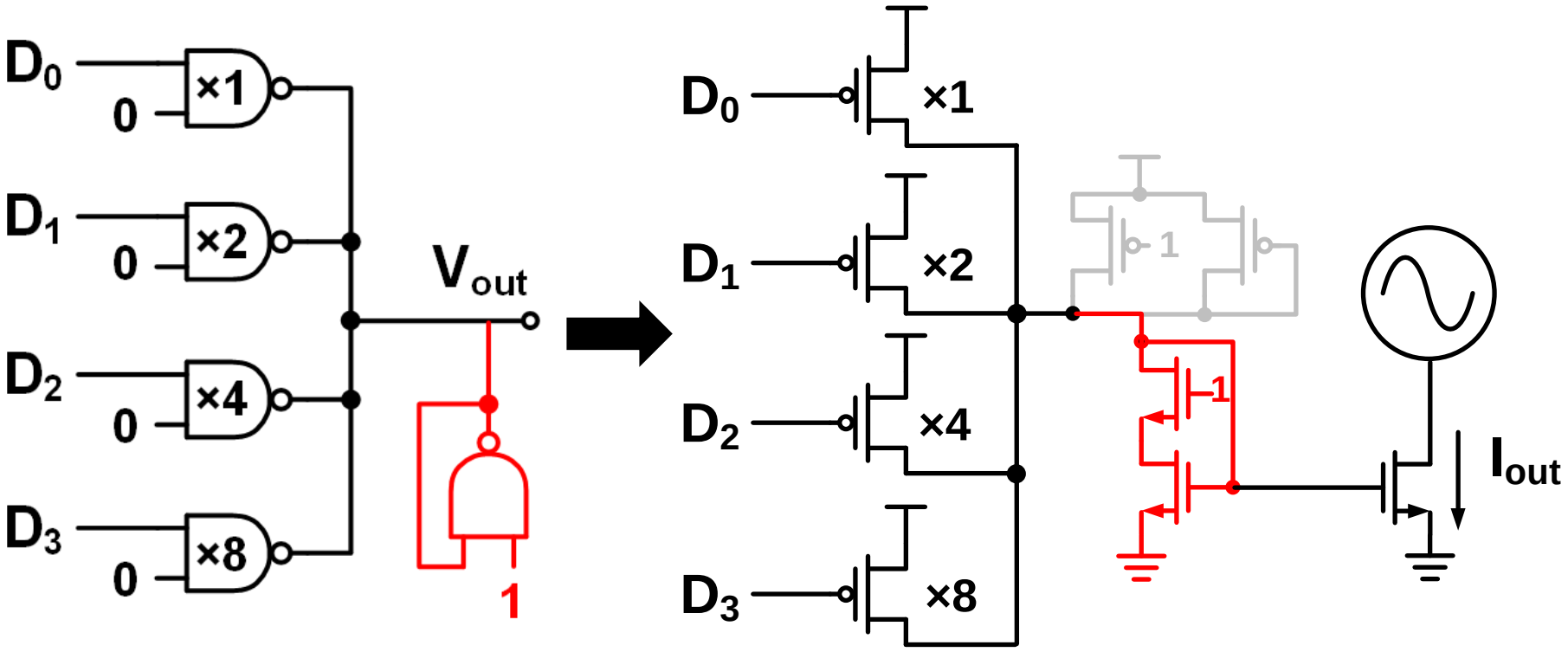
Coarse Tuning using DAC

Coarse tuning is made by current control

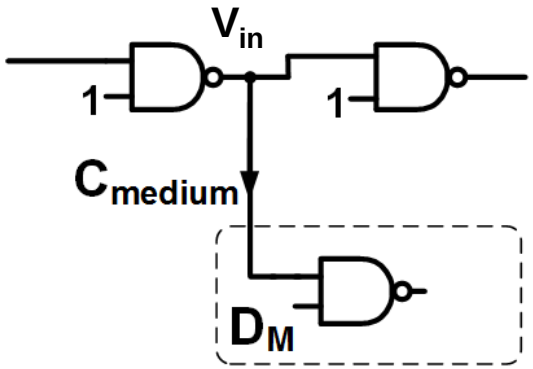


Proposed I-linear DAC

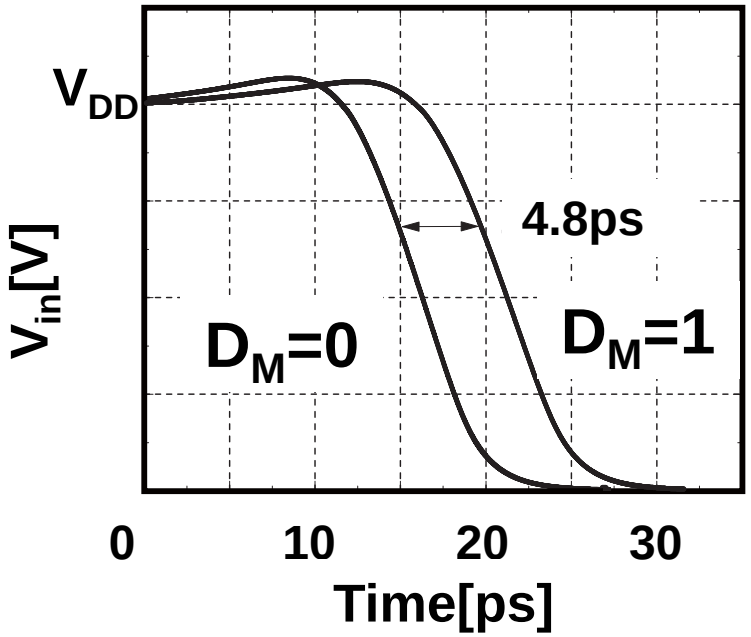
- A **feedback** for forming a current mirror.

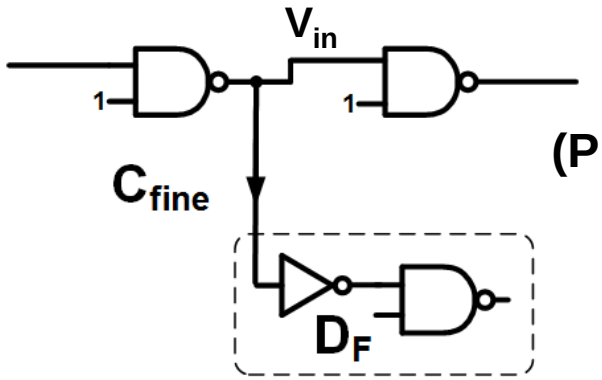


Tuning Capacitors



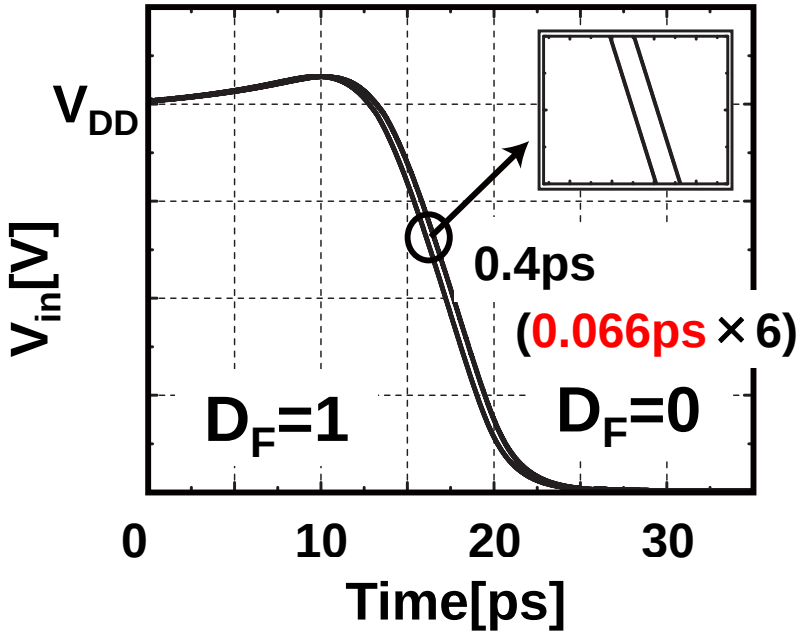
Medium resolution





(Proposed)

Fine resolution



High precision Time to Digital Converter

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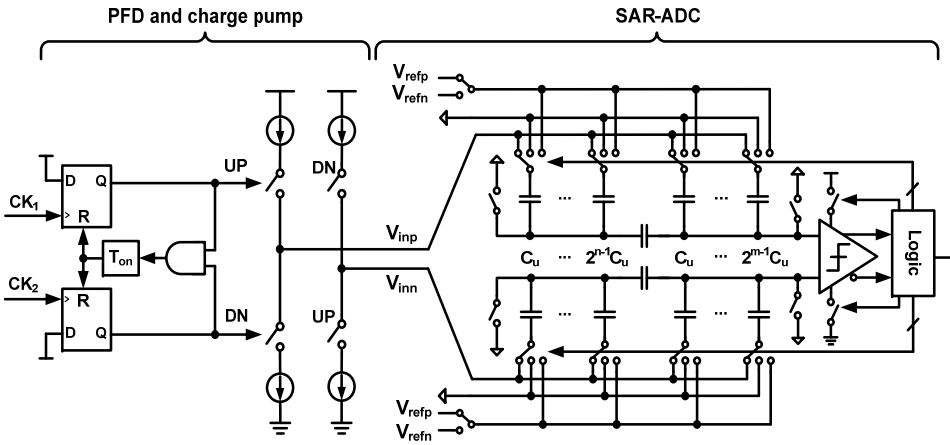
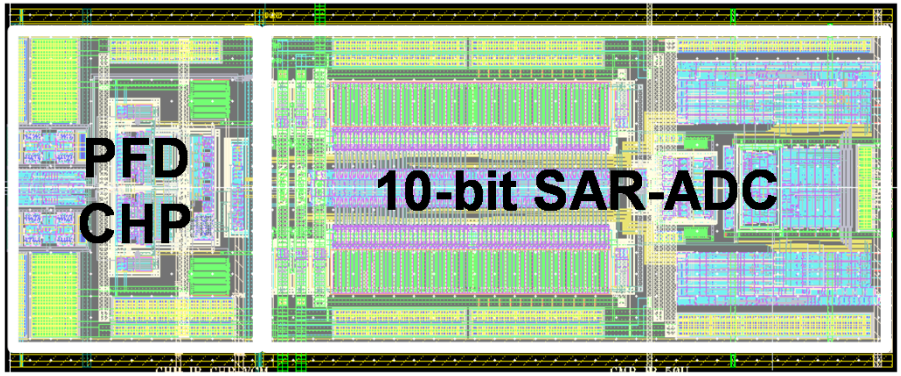
Charge pump + SAR ADC realizes sub-ps (0.8 ps) TDC
Resolution of conventional inverter based TDC is 10 ps at most.

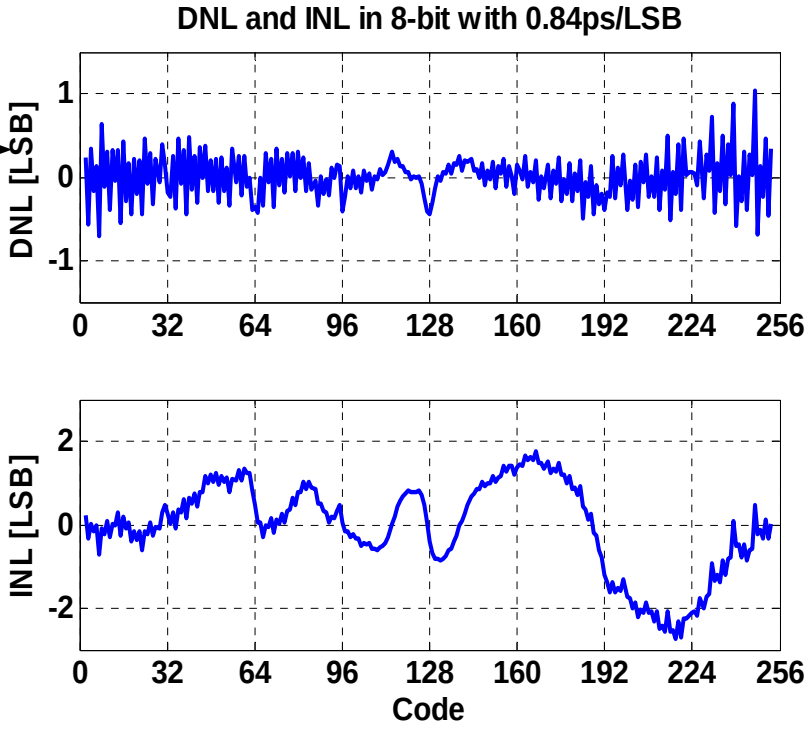
0.8ps, 10bit, 100Msps, 4mW, 0.02mm²





0.8ps, 10bit, 100Msps, 4mW, 0.02mm²

Low phase noise fractional PLL
On-chip jitter measurement
Sub-mm laser radar



Z. Xu, A. Matsuzawa, CICC 2013.

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