Automated design strategy for high performance mixed signal circuits

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Abstract

This paper discusses an automated design strategy for high performance mixed signal circuit. The reduction of the number of circuit types is firstly required for the smart automated design and addressing low voltage operation, scalability of power dissipation and performance are strongly recommended to select the circuits. A SAR ADC is reviewed as a strong candidate for the selected core of ADC. A fundamental issue of conventional layout method, place and lout are discussed. Advantage of MOM capacitor with pitch aligned layout with regularity is shown. The basic idea for the automated design flow in analog circuit design is proposed.

1. Introduction

Analog front-end circuits with mixed signal circuit cores; e.g. ADC, DAC, and PLL as shown in Fig. 1 will be needed for almost all electrical systems forever. However it becomes more difficult to obtain good circuit cores with sufficient performance, reasonable cost, and short development time. This is due to the increase of technical difficulty along with technology scaling, lack of matured circuit designer, expensive design tools, and increase of the simulation time.

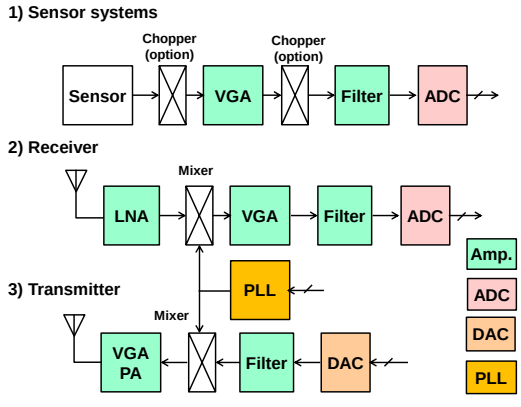

Fig. 1 Basic analog front-end circuits.

If we can't solve this issue, the progress of society that requires many sensing devices, communication devices, and IoT devices will slow down. This paper discusses the strategy for the realization of automated high performance mixed signal circuits to address this issue.

2. Basic strategy

The conventional issue to realize the automated design for analog circuits is due to the addressing all analog circuits without selection. The major required mixed signal circuits are ADC, DAC, PLL, VGA, Filter, at most and sometime mixer and power supply are added. For those core mixed signal circuits, we should make the following requirements.

1) Reduce the number of core circuit types.

The first step for automated analog circuit design is to reduce the number of core circuit types. The number of types of analog circuits is very larger than that of digital circuits and results in increase of difficulty of automated analog circuit design. Only the selected core circuits should be used for versatile applications.

2) Select the circuits that satisfy the following requirements.

The circuits can be used for the **low voltage operation**, since voltage lowering will continue with technology scaling and we should not change the circuit topology caused by design-rule change. The circuits have **small occupied area** to reduce the cost and should be **reducible with technology scaling**, since it is difficult to reduce the area for analog circuits and analog components, such as resistor, capacitor, and inductor. **Low power dissipation** is vital and the **power dissipation should be scaled** with the required performance, such as speed or bandwidth. The **layout pattern should have a regularity** to minimize the parasitic components and for the easy programming for automated layout. The **errors should be compensated by digital method** to guarantee the robustness of analog circuits.

3. Scalable SAR ADC

A SAR ADC is widely recognized as a most energy efficient and small size ADC with moderate resolution and moderate conversion speed. In this chapter, a SAR ADC will be reviewed as strong candidate for the selected core. Fig. 2 shows our developed 12 bit SAR ADC [1]

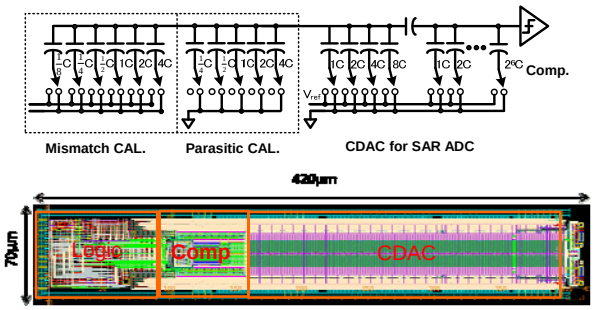

Fig. 2 12 bit SAR ADC.

It consists of only capacitor array, dynamic comparator and logic circuits. The CDAC uses split capacitor to reduce the capacitor ratio and to minimize the occupied capacitor area. The mismatch of capacitance can be compensated by mismatch calibration circuit and also the conversion error caused by mismatch between the split capacitance and attenuation capacitance can be compensated digitally.

The capacitors dominate the area of circuit and we used MOM capacitance that uses capacitance between the interconnect metals, as shown in Fig. 3.

This is an important technology choice. The MIM capacitor has been used for the analog circuit, since the accuracy is better than MOM capacitance. However the extra process steps are required and the density will not increase with technology scaling. It results in increase of cost and decrease of performance due to relatively large parasitics. The MOM capacitor has no excellent accuracy; however we can address this issue by using the digital linearity compensation.

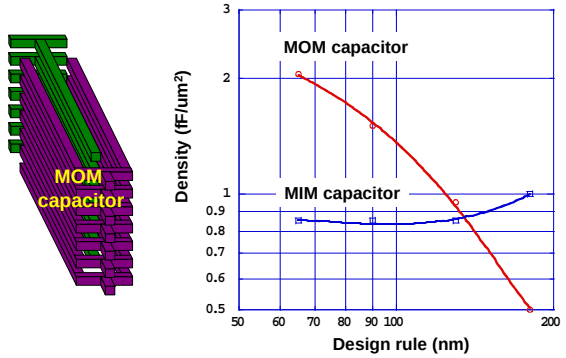

Fig. 3 MOM capacitor and capacitance density.

The density of the MOM capacitor can be increased by technology scaling, as shown in Fig. 3.

This can reduce the occupied area when using more scaled technology and the cost of the analog circuits will not increase.

The comparator, shown in Fig. 4 is a dynamic circuit like logic gate. No static current flows. The circuit uses the differential flip-flop, however takes care of noise reduction to realize the high effective resolution [2].

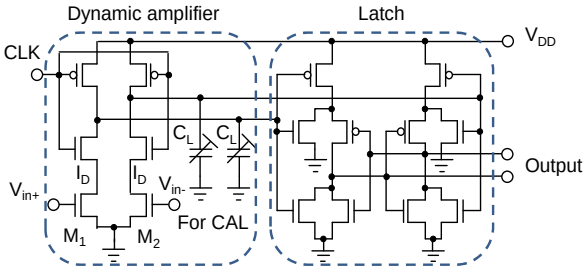

Fig. 4 Low noise dynamic comparator.

The ADC does't need an external high frequency clock, since it uses self-clocking technique. Fig. 5 shows the conversion timing. The successive conversion is started after the sampling is finished. The self-clocking circuit generates high frequency pulses for the SAR conversion and stops after counting 12 pulses. The End flag is generated to indicate the finish of the conversion and it can be used to reduce the leakage current by the power gating.

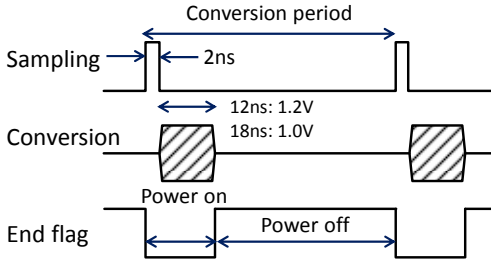

Fig. 5 Conversion timing diagram.

Fig.6 shows measured power dissipation as a function of the sampling frequency. The ADC can be operated up to 70MS/s with power dissipation of 4.5mW.

The power dissipation is proportional to the sampling frequency like the digital logic circuit. Therefore the power dissipation is scalable with conversion frequency and it can be reduced so much; such as 200uW at 5MS/s, 20uW at 500KS/s, 2uW at 50KS/s, if the leakage current is shut off by power gating. Low voltage operation, such as 0.8V power supply is possible and it can be used in more scaled technology. This characteristics is very

suitable for versatile use; such as for wireless communications and IoT sensing systems.

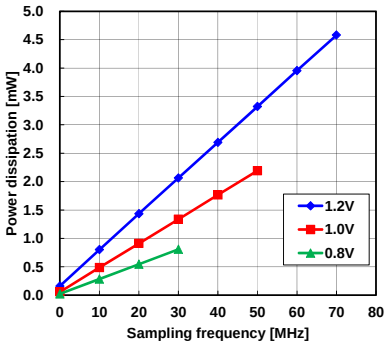

Fig. 6 Power dissipation vs. sampling frequency.

This ADC has the performance scalability for the versatile use. Fig. 7 plots the performance of published ADCs for wireless communication [3] and shows the measured SNR of the developed SAR ADC for the signal bandwidth

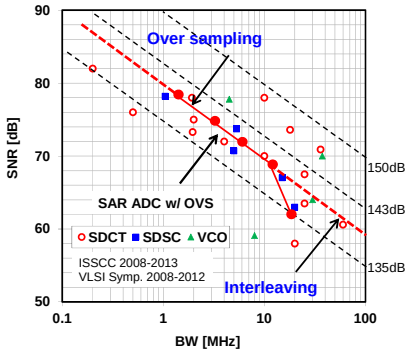

Fig. 7 performance of published ADCs for wireless communication and measured SNR of developed SAR ADC for the signal bandwidth.

The SAR ADC with digital LPF demonstrates the realization of sufficient SNR for the signal bandwidth. It suggests us that only one SAR ADC is enough for many wires standards. The interleaving can increase the signal bandwidth over the 20MHz.

Fig. 8 shows the power dissipation of published ADCs for wireless communication and the developed SAR ADC. The power dissipation of the developed ADC is the lowest for all published ADCs in wireless communications.

4. Layout driven circuit design and automated layout

Layout of analog circuits affects the performance so much.

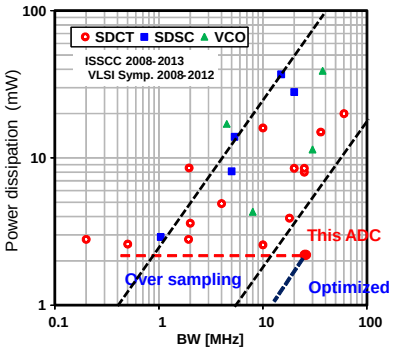

Fig. 8 Power dissipation of published ADCs for wireless communication and developed SAR ADC.

Fig. 9 shows a layout issue of SAR ADC that we made. In this design, we used MIM capacitors and connected them with interconnection metals and the parasitic capacitance of 3.5F is made between the top plate line and MSB line. It caused a large conversion error that can't be compensated.

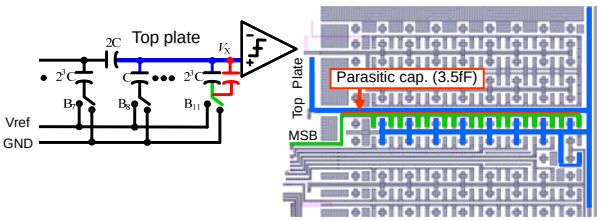

Fig. 9 Layout issue of SAR ADC.

A conventional layout method of IC design is "place the components and rout them" as shown in Fig. 10.

This method essentially makes harmful parasitic components caused by routing wires.

To avoid parasitic components, we should not separate the components and routing wires, but unify them.

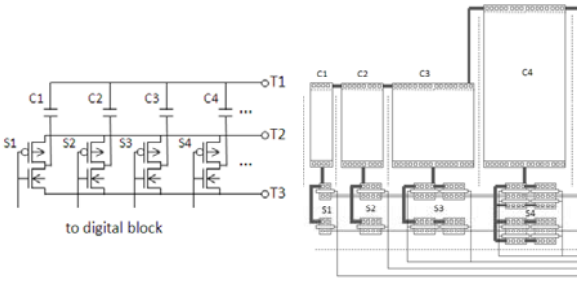

Fig. 10 Conventional layout method: Place & Route.

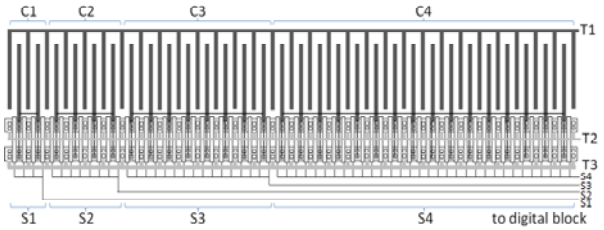

Fig. 11 Proposed layout method.

Fig 11 shows our proposed layout method. MOM capacitors with equal pitch are used to avoid routing wires and the pitch of switch is adjusted to keep the regularity.

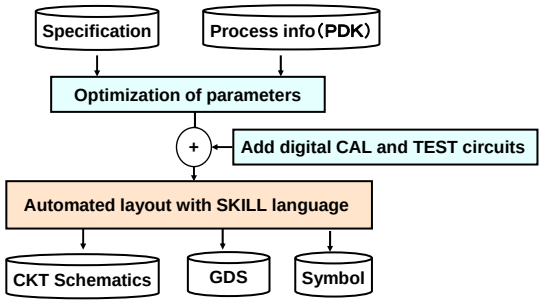

Fig. 12 Proposed design flow for mixed signal circuits.

We are now developing new design flow for mixed signal circuits, as shown in Fig. 11. The users are required just to input the specification of the circuits. The PDK is prepared and the parameters are determined by the parameter optimizer. After adding the digital calibration and testing circuits, the automated layout system using SKILL language generates the GDS, symbol, and schematics, automatically.

Fig. 13 shows the layout of resistive DAC, as an example of this automated circuit design system. The pitch aligned layout makes automated layout easier and the occupied area and power dissipation can be minimized and the speed can be increased.

This automated design system addresses only the circuit having regularity in the layout for realizing high efficient programmability.

5. Summary

Automated design strategy for high performance mixed signal circuit is discussed. The reduction of number of circuits is important and addressing low voltage operation, scalability of power dissipation and performance are strongly required. Developed SAR ADC is reviewed as a strong candidate for selected core. A fundamental issue of conventional layout method, place and lout are discussed. Advantage of MOM capacitor with pitch aligned layout with regularity is shown. The basic idea for automated design flow for analog circuit design is proposed.

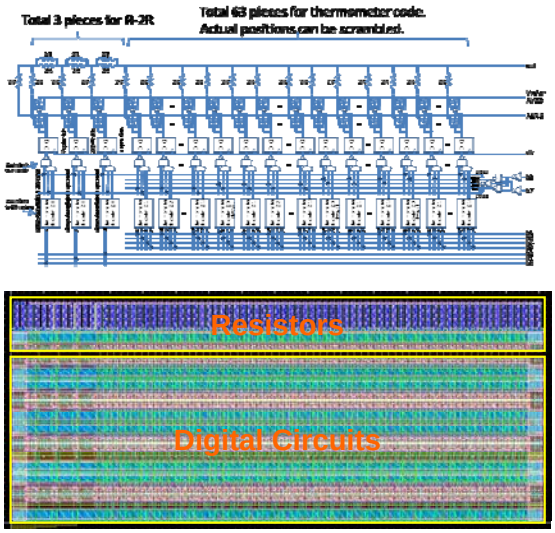

Fig. 13 Resistive DAC; Circuit schematic and layout generated with automated analog layout design.

References

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