A Novel Direct Digital Frequency Synthesizer Employing Complementary Dual-Phase Latch-Based Architecture

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Outline

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- Motivation
  - Digital TV VHF/UHF/L/S Bands
  - Issues of Direct Polar Modulator
- Background
  - Direct Digital Frequency Synthesizer
  - Complementary Dual-Phase Method
- Proposed DDFS architecture
- Results
- Conclusion

Motivation

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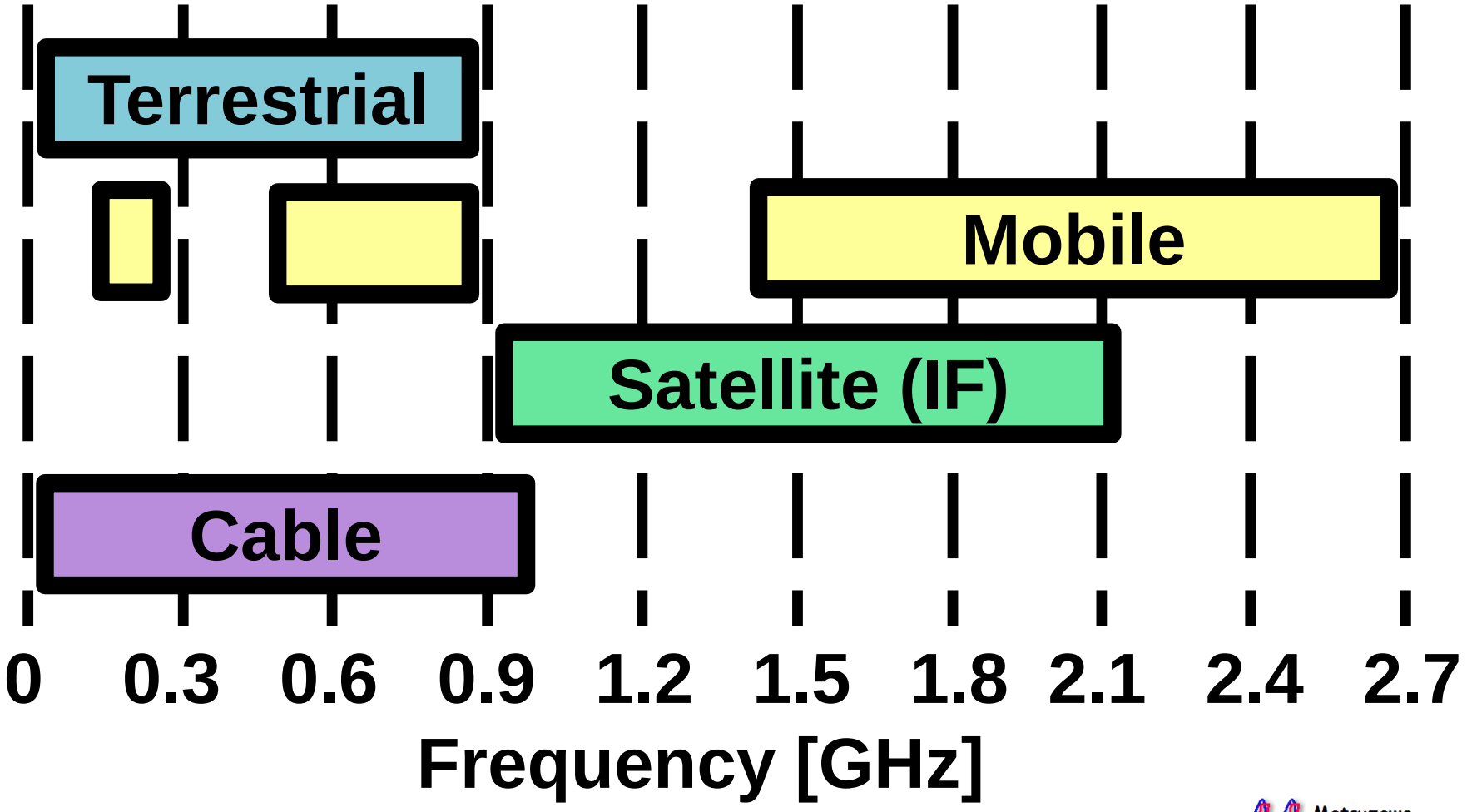
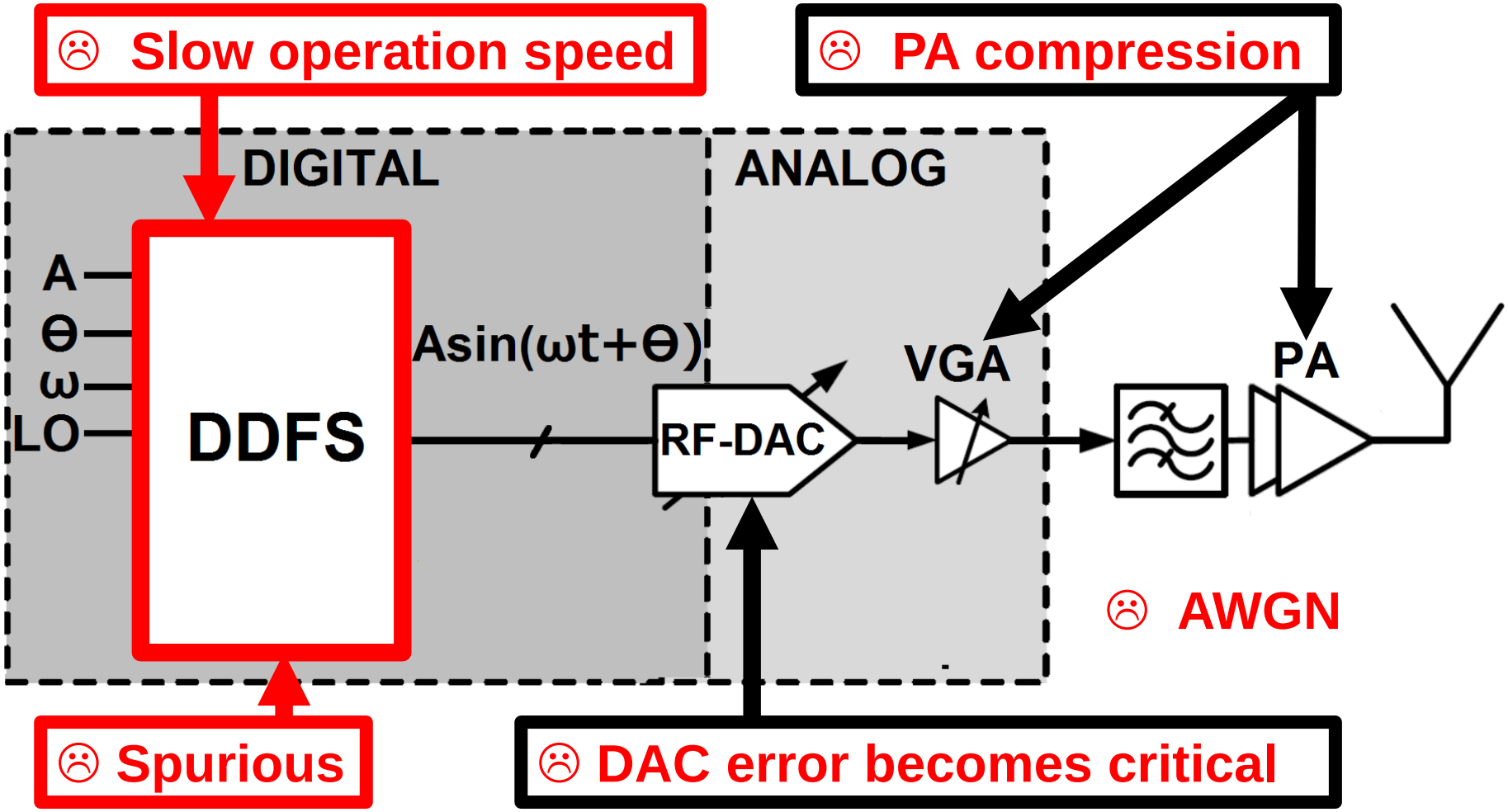
Digital TV VHF/UHF/L/S Bands:

Integrated All-standard Modulator hasn't been reported yet.



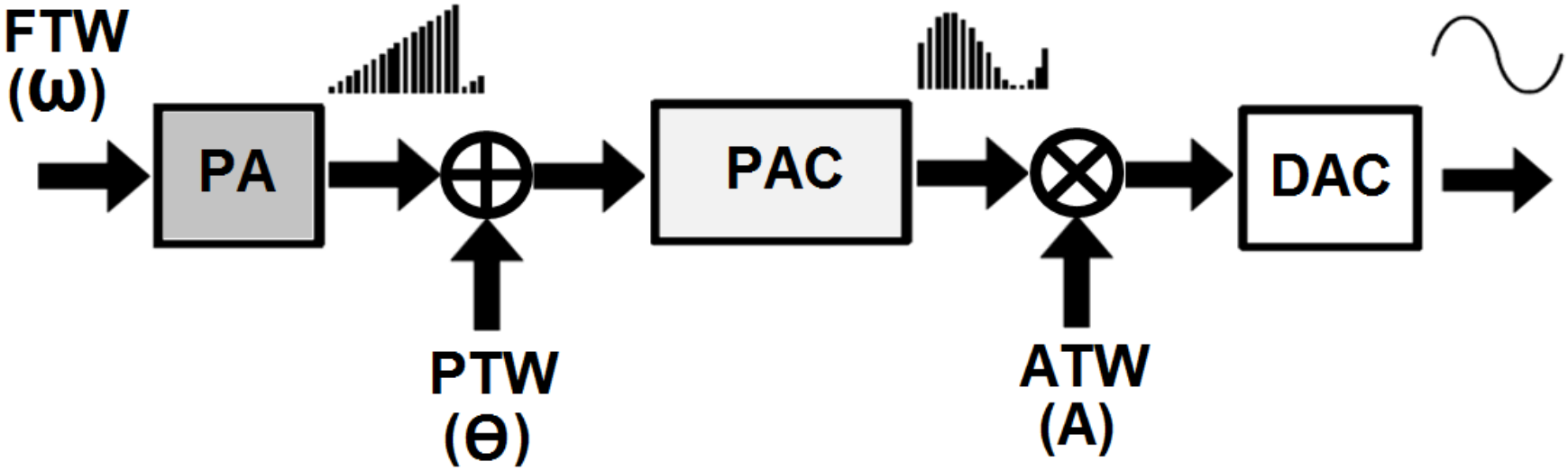
Motivation

Issues of Direct Polar Modulator:



Background

Direct Digital Frequency Synthesizer:

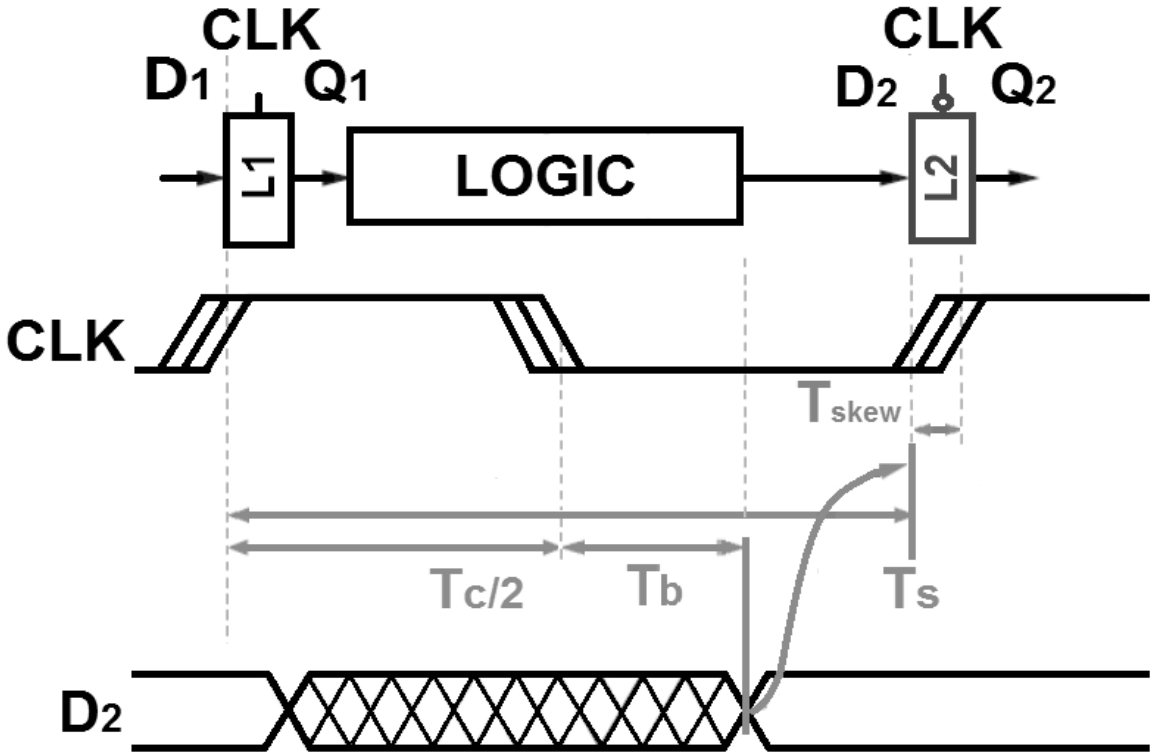


$$DDFS_{out} = A*\sin(\omega t + \Theta)\ [1]$$

Background

Complementary Dual-Phase Method:

"Borrowing" time relax timing requirements



$$T_b \leq T_c/2 - (T_s + T_{skew}) \text{ [2]}$$

Proposed DDFS architecture

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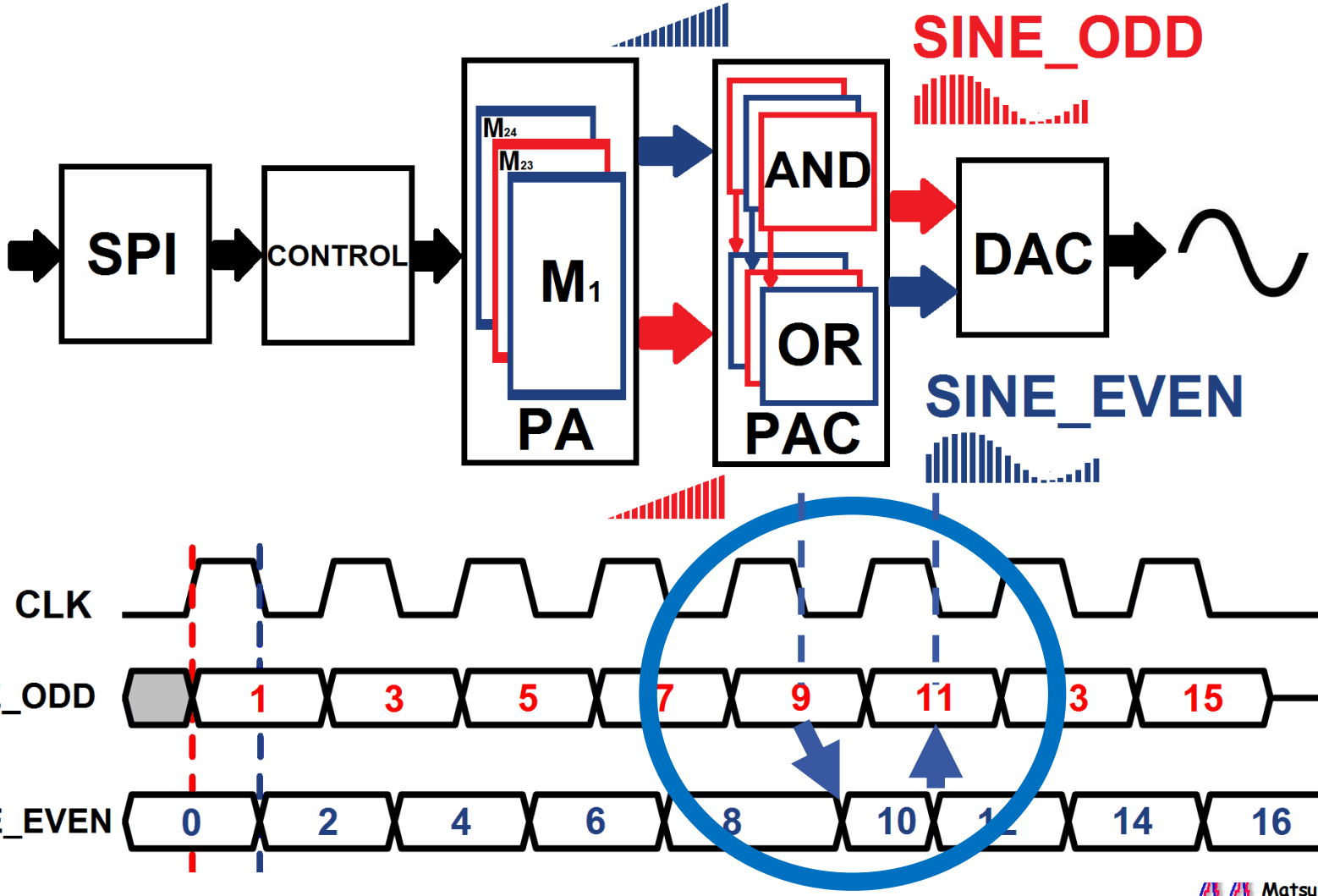
Allows double data rate and time borrowing



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Proposed DDFS architecture

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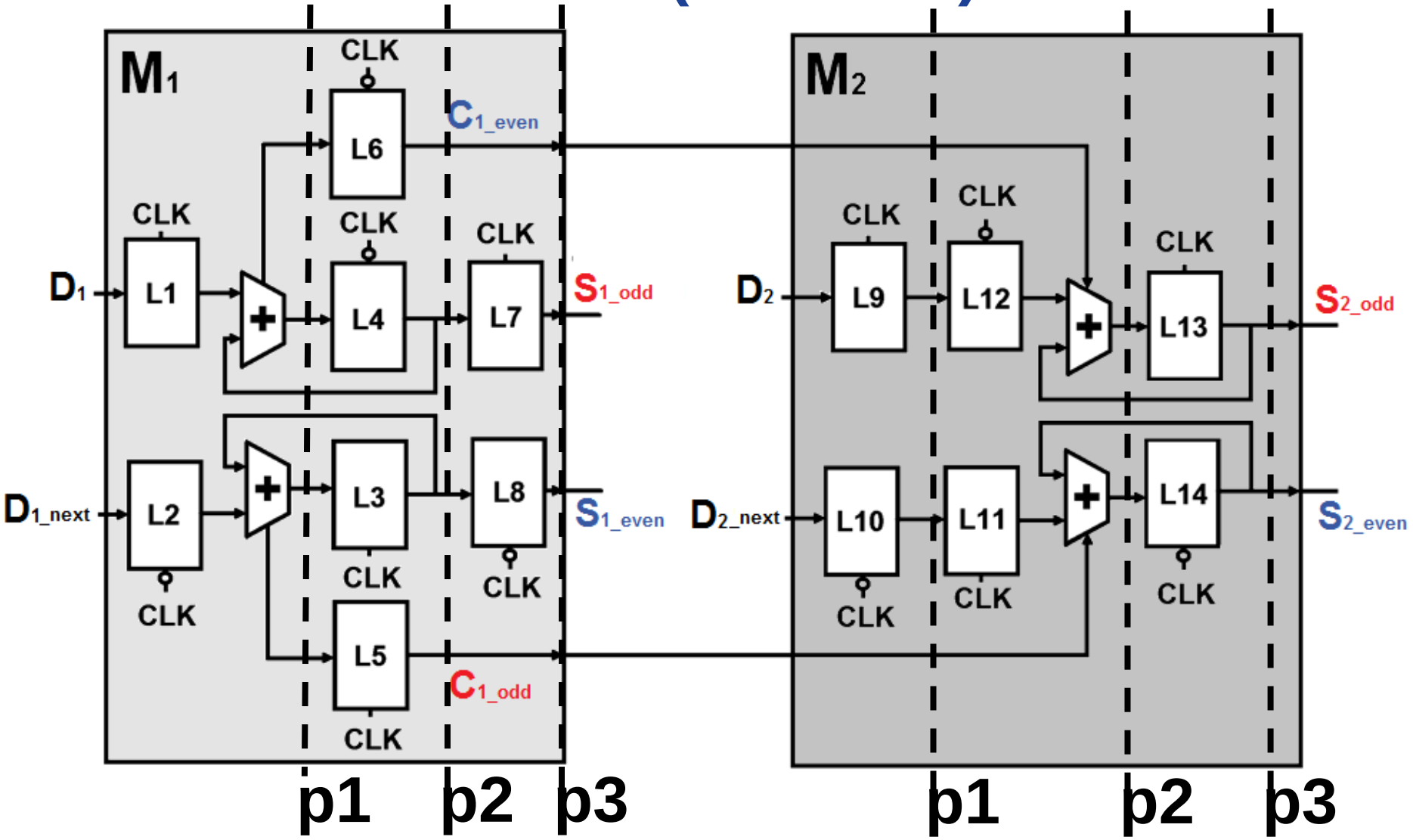
Phase Accumulator (PA 2 bits) :



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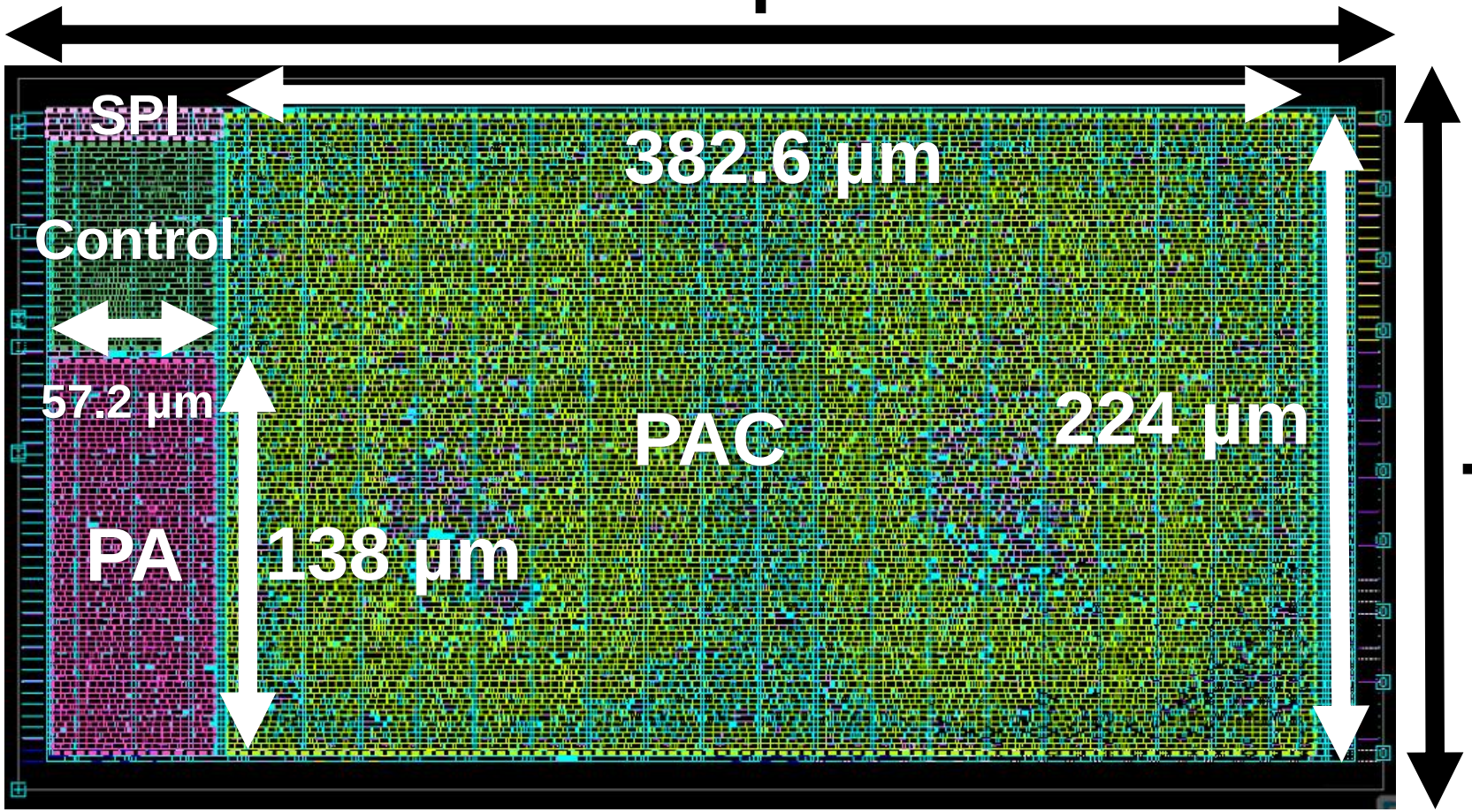
Results

Floorplan view

Core size is 0.1mm², comprising 25614 cells



Results

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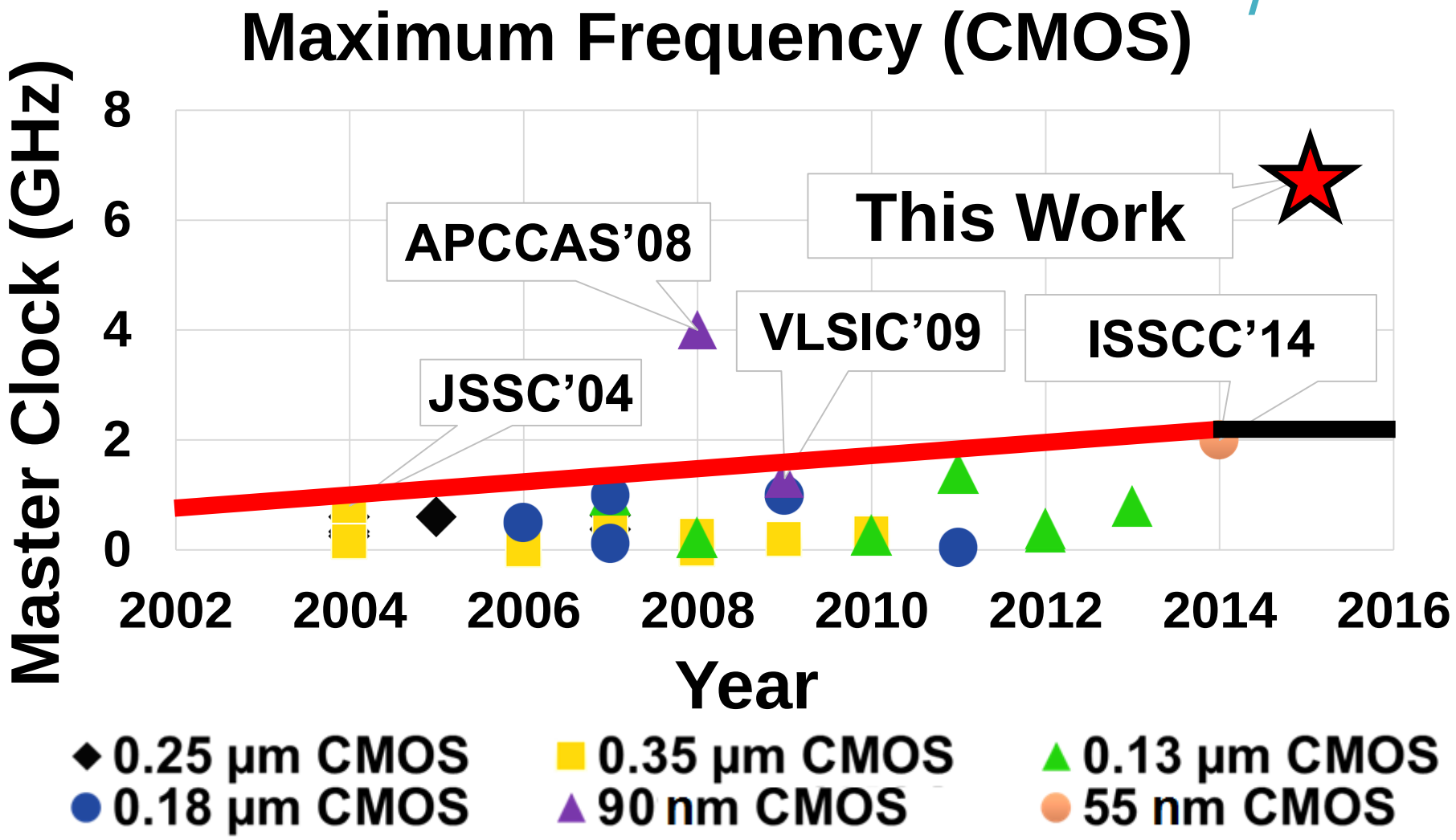
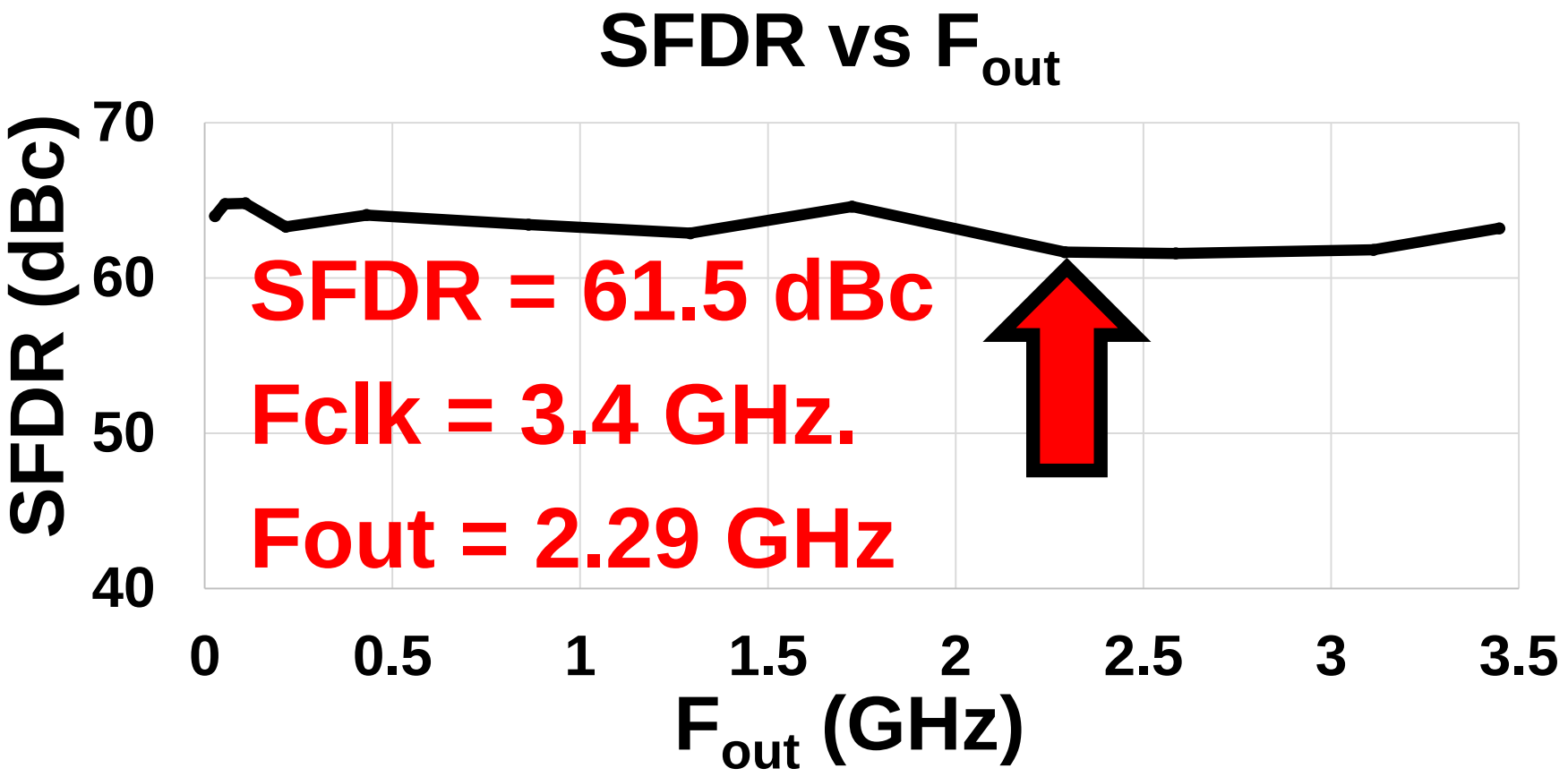


Results

SFDR Performance:

Expected worst case SFDR is 61.5 dBc



Results

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Performance Comparison:

Fastest CMOS DDFS performance is expected

Reference	Architecture	T	A	CMOS Technology	Sampling Rate (GS/s)	Area (mm^2)	PE (W/GS/s)	SFDR (dBc)
This Work (Simulated)	Digital Mapping	24	10	65 nm	6.8	0.1	0.022	61.5
ISSCC'14 [8] (Measured)	Nonlinear DAC	32	9	55 nm	2	0.1	0.065	55.1
TCSI'11 [7] (Simulated)	Digital Mapping	24	9	0.13 µm	1.4	0.006	0.005	62
VLSIC'09 [6] (Measured)	Nonlinear DAC	24	11	90 nm	1.3	2	0.26	52
APCCAS'08 [5] (Simulated)	Nonlinear DAC	12	7	90 nm	4	N/A	0.1155	44
JSSC'04 [4] (Measured)	Digital Mapping	32	9	0.35 µm	0.8	1.47	0.217	55

Conclusions

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1. First Complementary Dual-Phase Latch-Based DDFS core has been proposed.
2. A maximum data sampling rate of 6.8 GS/s and 0.022 W/GHz power efficiency is expected.
3. The proposed DDFS can potentially cover VHF/UHF/L/S Bands: 50 MHz - 2660 MHz.
4. Integrated All-standard Modulator for Digital Television can be implemented by using this system.

References

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